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INTEGRATED CIRCUIT
ELECTROMAGNETIC SUSCEPTIBILITY
INVESTIGATION - PHASE II

TEST AND MEASUREMENT SYSTEMS

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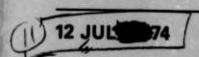


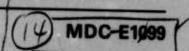
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## INTEGRATED CIRCUIT **ELECTROMAGNETIC** SUSCEPTIBILITY INVESTIGATION

PHASE IL.





TEST AND MEASUREMENT SYSTEMS.



Test and Evaluation;

SUBMITTED TO: CONTRACTING OFFICER U.S. NAVAL WEAPONS LABORATORY DAHLGREN, VA. 22448 CONTRACT NO. NG6178-73-C-9362



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#### PREFACE

This document is one of eight task-oriented reports prepared under Contract No. N00178-73-C-0362 for the U. S. Naval Weapons Laboratory, Dahlgren, Virginia 22448. The McDonnell Douglas Astronautics Company Personnel involved were:

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### INTEGRATED CIRCUIT SUSCEPTIBILITY

#### TABLE OF CONTENTS

	<u>Title</u> <u>Pa</u>	age
1.	INTRODUCTION AND SUMMARY	1
2.	TEST FIXTURES	2
	2.1 Flat Pack Test Fixture 2.2 Dual In-Line Package Test Fixture 2.3 TO-5 Package Test Fixture 2.4 Bias Unit	3 3 4 5
3.	SEMI-AUTOMATED TEST SYSTEM	7
	3.2 RF Test Fixture Calibration 3.3 Interference Testing Using the Semi-Automatic Test System 3.3.1 7400 NAND Gate Interference Testing 3.3.2 741 Operational Amplifier Interference Testing 3.3.3 MOS 4011 Interference Testing 3.3.4 2002 Hybrid Interference Testing 3.3.5 Extra Digital Device Interference Testing 3.4.1 Digital Control Box 3.4.2 Operational Amplifier Control Box 3.4.3 MOS Control Box 3.4.4 Comparator Box 3.4.5 Comparator Control Box 3.4.6 Voltage Regulator Control Box	1 1 2 2 2 3 3 3 3 4 4
4.	CATASTROPHIC FAILURE TESTING	5
DIS.	TRIBUTION LIST	2

#### LIST OF PAGES

Title

i - ii

1 through 156

#### 1. INTRODUCTION AND SUMMARY

This report describes the RF test fixture and the semi-automatic test set up developed on contract number N00178-73-C-0362 to investigate the susceptibility of integrated circuits to high power RF signals. Some of the material contained herein has appeared in previous reports, but is also included here to provide a complete testing document.

Test fixtures were fabricated to permit testing of integrated circuits with up to 16 leads on three different package styles (flat-pack, dual in-line, and TO-5 can) while fully biased and operational. The semi-automatic test system was developed to facilitate collecting the enormous amount of data needed for the integrated circuit susceptibility investigation. The heart of the system is an HP9810A programmable calculator and a 50-channel scanning digital voltmeter; however, several circuits had to be designed and fabricated to aid in biasing and loading the IC and to interface with the computer.

To facilitate reading, figures start on page 16 and tables start on page 74.

#### 2. TEST FIXTURES

Development of suitable test fixtures and a semi-automatic test system to assist in collection and recording of data was a key achievement of this program. This section describes the test fixtures and the principles used in their design. Design of the test fixtures incorporated the following requirements:

- (1) interface the IC with conventional RF transmission lines
- (2) provide operational conditioning for biased testing of ICs
- (3) permit determination of dissipated RF power within the IC to an absolute accuracy of 10%
- (4) exhibit a bandwidth of 100 MHz to 12.4 GHz
- (5) permit repeatable measurements.

A test fixture for each of the three package styles (flat-pack, dual in-line, and TO-5 can) is now available. In an earlier report we had indicated an approach involving a universal base module containing the RF input lines and having bias units incorporated into each line to separate the video and RF frequencies. After further consideration, we decided that the advantages associated with having more than one complete test fixture available outweighs the small cost savings associated with the universal base module concept. Consequently, a complete test fixture is available for each package style.

Each fixture features stripline technology to interface between the IC package and conventional RF transmission line. Stripline launchers accomplish the transition from coaxial transmission line to the stripline paths on the board. Type N connectors provide standard, reliable, well shielded RF connections. Such connection ease expedites measurements at all ports. The video inputs to the test fixture are through type BNC connectors. Paragraphs 2.1, 2.2, and 2.3 describe the test fixtures for the flat-pack, dual in-line, and TO-5 can packages, respectively. The bias units are the same for all the test fixtures and are described in paragraph 2.4



2.1 Flat Pack Test Fixture - Figure 1 is an exploded view of the test fixture which will accommodate flat pack ICs having up to 16 leads. Items (19) and (20) form the stripline feed system (consisting of two copper clad, low loss tangent, dielectric boards). The bottom board has the stripline paths etched upon it. Installation holes in the centers of the top dielectric board and cover plate permit the IC to be placed within the fixture. An IC lead locater plug, item (15), taken from an integrated circuit test socket is press fitted into the center of the bottom dielectric board. It holds the device in a consistent orientation which assures proper alignment of the leads.

A cover plug, item (12), fits snugly into the installation hole enclosing the IC within the stripline feed system. The cover plug also provides dielectric continuity above the device and RF shielding integrity for the top aluminum cover plate. By applying pressure upon the IC leads which lay atop the stripline feed system in the fixture, the cover plug connects the IC to the stripline. Rubber pads, item (13), evenly distribute the pressure to all IC leads. A toggle clamp, item (4), provides an adjustable pressure to enable a reliable connection.

Structural rigidity is required of the fixture to permit repeatable data. Consequently, the stripline boards are enclosed in an aluminum housing which keeps the dielectric boards from flexing or moving. Screws shorting the two ground planes together are located at intervals of less than one-half wavelength at the highest frequency of interest to prevent propagation of higher order modes.

The bias units, item (27), are connected to the stripline type N launchers and are held in place by the test fixture skirt, item (22). The lower connector on each bias unit is the RF input (or output) and is DC isolated from the IC. DC bias and video pulses can be applied or measured using the upper connector on each bias unit.

2.2 <u>Dual In-Line Package Test Fixture</u> - Figure 2 is an exploded view of the test fixture which will accommodate dual in-line packaged ICs having up to 16 pins.

Items (10) and (11) form the stripline feed system. The top board has the stripline paths etched upon it. A 16 pin dual in-line socket, item (8), is used to assure a consistent orientation of the IC under test. The copper on the ground plane side of the top board has been removed from under the socket and holes drilled through the dielectric board for the 16 pins from the socket. Each pin is soldered to the appropriate stripline center conductor. The socket is held securely in place by small tabs, item (6), bolted to the top plate of the aluminum housing. The cover plug, item (1), and spring loaded hold down, item (2), assures RF shielding integrity for the top plate. Removal of the IC is facilitated by a lever, item (18), and two small teflon rods, item (19).

Structural rigidity is obtained in the same manner as for the flat pack package test fixture. Bias units are connected and used in the same way as for the flat pack package test fixture.

2.3 TO-3 Package Test Fixture - The TO-5 package test fixture was designed to accommodate TO-5 cans having 8 or 10 pins. Figure 3 is an exploded view of the test fixture. Items (9) and (10) from the stripline feed system. The top board has the stripline paths etched upon it. Two interchangeable top boards are required; one for 8-pin TO-5 packages, another for 10-pin packages. A socket, item (7), is used to assure a consistent orientation of the IC under test. A test cap, item (6), provides alignment guides for the pins to facilitate placement of the IC into the socket. The copper on the ground plane side of the top board has been removed from under the socket and holes drilled through the dielectric board for the socket pins. Each pin is soldered to the appropriate stripline center conductor. The test cap and socket are held securely in place by the aluminum housing, with the top plate contacting the lip around the bottom of the test cap. The cover plug, item (1), and spring loaded hold down, item (2), assures RF shielding integrity for the top plate. Removal of the IC is facilitated by a lever, item (21), and a small teflon rod, item (13).

Structural rigidity is obtained in the same manner as for the flat pack package test fixture. Bias units are also connected and used in the same way.

2.4 <u>Bias Unit</u> - The function of the bias insertion unit is to provide a low-pass path for the video signals while providing high-pass characteristics for the RF signal. The problem is complicated by the wide RF frequency band (100 MHz to 10 GHz) over which the unit must perform. Desirable video section performance is free passage of video signals up to approximately 10 MHz while rejecting RF signals by approximately 20 dB. The RF section must provide RF transmission properties with no large reflections due to mismatches in the line, especially near the video section connection. The basic design requires a capacitor (DC block) in the RF line to reject low frequency signals and an inductor (RF choke) in the video line to reject high frequency signals. Achieving a good RF choke in the microwave region is difficult across a wide band due to resonances in interwinding capacitances or distributed parameters. The use of ferrite material as a core offered the best chance for success.

After considerable development, success was achieved with the design diagrammed in figure 4. A 2 1/2 turn choke on a ferrite core provided the RF choke while a commercial DC block (coaxial) is used in the RF line to isolate low frequency signals. Figure 5 is a cutaway drawing of the assembled bias unit.

This bias unit provides a nominal 20 dB isolation from the RF path to the bias input port, passes a one microsecond, one ampere pulse with an 80 nanosecond risetime from the bias port to the test IC, and has an RF path insertion loss of 3.5 dB or less. Figure 6 shows the measured insertion loss from the RF path to the bias input port. Figure 7 shows the measured RF insertion loss through the RF path.

Figure 8 shows the setup used to measure the video path response to short, high current pulses. Figure 9 compares the open circuit voltage available from the pulse generator to the received pulse at the test device port. At current levels up to

one ampere, no ferrite saturation effects are seen, and the risetime is shown to be approximately 80 nanoseconds. Protection offered to the RF generator by the DC block is shown in figure 10. Table 1 lists the data for loss calibration for the 16 bias units used for the interference testing.

#### 3. SEMI-AUTOMATED TEST SYSTEM

To facilitate collecting the enormous amount of data needed for the integrated circuit susceptibility investigation, MDAC-E developed a semi-automatic test system specifically for use on this contract. The heart of the system is an HP9810A programmable calculator and a 50-channel scanning digital voltmeter. Data is recorded on a digital tape cassette for later processing in an HP9830A computer. The following paragraphs describe the test set ups, test procedures, computer programs, and peripheral equipment designed and fabricated to aid in testing the various types of integrated circuits.

3.1 <u>Crystal Detector Calibration</u> - One of the critical tasks in setting up the semi-automatic test system was the calibration of the crystal detectors to permit determination of RF power level at each port of the test fixture during a test. A test requires monitoring the power entering one port and exiting from as many as 16 ports (the other 15 pins on the IC plus the reflected power from the input port). Seventeen HP423A crystal detectors were calibrated by subjecting them to sequential steps of RF power while monitoring the detected voltages. Each crystal detector was terminated in a 10K ohm resistor. This value was chosen as a compromise for obtaining adequate detected output voltage while not appreciably affecting rise and fall times during testing for pulsed conditions.

Calibrations were performed at all five test frequencies (.22, .91, 3.0, 5.6 and 9.1 GHz). The data was processed to obtain a least squares fit to the equation:

$$y = B_0 + B_1 x + B_2 x^2 + B_3 x^3$$

where:  $y = \log_{10} (RF power)$ 

 $x = log_{10}$  (detected voltage)

and  $B_0$ ,  $B_1$ ,  $B_2$ , and  $B_3$  are the calculated coefficients. The cubic-order power-series-fit proved to be quite adequate over the power range of .01 to 100 milliwatts required

for testing after accounting for the various coupling and attenuation factors associated with each port. Table 2 shows a typical data tabulation where the actual and calculated values are compared. Figure 11 shows a graph of a typical calculated function and the measured data points. Tables 3 through 7 show the values of the coefficients which are used by the HP9810A calculator to compute the various power levels as the detected voltages are measured.

Figure 12 shows the data acquisition and recording set up for the crystal detector calibration. Figures 13 through 17 are block diagrams of the RF portions of the crystal calibration test set ups for each of the five test frequencies. The HP9810A program used to acquire and record the crystal detector calibration data is shown in table 8. The recorded data at this stage is not in array format. To change the data to an array format, which is desirable for data reduction by the HP9830A, and to obtain a hard copy of the data, the recorded data was then processed on the HP9830A computer calculator, using the program shown in table 9, and recorded. The program shown in table 10 was then used in calculating the calibration coefficients on the HP 9830A.

3.2 <u>RF Test Fixture Calibration</u> - Each test fixture was characterized for dissipation loss without bias units. Dissipation loss is a measure of the fraction of RF power lost from a given path within the fixture. That fraction of power not dissipated in the fixture or coupled out of the ports must be delivered to the IC. Fixture dissipation had to be determined accurately, since a knowledge of power dissipation within the device to an absolute accuracy of +10% was desired.

Dissipation losses are primarily due to characteristics of the stripline paths within the fixture. The dissipative loss per stripe, L, is defined as the ratio:

$$L = \frac{P_{in}}{P_{out}} > 1$$

where Pout is the power delivered at the end of the stripe for an input power Pin.

Since each stripe is the same length and shape, L is assumed to be the same value for each of the istripes. This assumption was verified experimentally.

Referring to figure 18, the power which comes out of each port must be L times greater at the center of the fixture. Hence, P<sub>dist</sub>, the total power distributed from the center, is given by:

$$P_{dist} = \sum_{j=1}^{i} p_{j}$$

P is the amount of power available for distribution from the center of the fixture and is given by:

 $P_a = \frac{P_{incident}}{L}$ 

Conservation of energy requires that these two quantities be equal. Hence:

$$P_a = P_{dist}$$

and,  $L^2 = \frac{P_{incident}}{\Sigma P_i} \qquad (j = 1 \rightarrow i)$ 

It is not possible to measure directly the loss per stripe because of lack of connectors at the IC end of each stripe. A dummy IC was made for each test fixture which shorted stripes together so that a continuous path was provided between ports.

By using each port for power input to the fixture at each given frequency, i different values of L were measured for each fixture. Statistical analyses were performed on this group of loss factors to compute the average loss and the standard error. The test fixture calibration was performed using the semi-automatic test system. In operating the system for test fixture calibration, the operator initiates the data cycle by pressing the CONTINUE button on the HP9810A calculator. The system sequentially samples the RF power level of the required number of ports by means of the calibrated crystal detectors and records the data. The operator then changes the input ports, presses the CONTINUE button again, and more data is acquired and recorded. This process is repeated until all ports have been used as

input ports. The HP9810A then calculates and prints out (on a typewriter) the calculated loss when using each port as an input, the mean loss and the standard error (all in dB).

Figure 19 shows the data acquisition and recording set up for test fixture calibration. Figures 20 through 24 are block diagrams of the RF portions of the test set ups. Table 11 is a listing of the HP9810A program for the test fixture calibration and table 12 lists the data register allocations for that program.

Tables 13 through 17 show the data resulting from the measurements and calculations for the 16 pin dual in-line package test fixture. Tables 18 through 22 are the results for the 8 pin TO-5 package test fixture.

3.3 Interference Testing Using the Semi-Automatic Test System - The semi-automatic test system is illustrated in figure 25. Acquisition and storage of the data in the laboratory is controlled by an HP9810A claculator. It also directs the data recording on digital tape cassettes. Analysis of this data is performed using an HP9830A computer. A hard copy of the data, an example of which is shown in table 23 is prepared to verify successful data runs and as insurance against mishap with the tape. The computer is also used to prepare curves such as shown in figure 26, thus providing a pictorial representation of the data to aid in analysis.

In operating the semi-automatic test set-up for interference testing, the operator selects an input power level to be applied to the device and initiates the data cycle by pressing the CONTINUE button on the HP9810A calculator. The system sequentially samples the RF power level of the required number of ports by means of the calibrated crystal detectors, computes the ratio of power delivered to the device to the input power (the calibration factor) using a stored program and constants, then measures various device voltages and currents. Selected device voltages and currents and the calibration factor are stored along with the corrected power dissipated in the chip (which is the independent variable) on the digital tape cassette. A photograph of the system in operation is shown in figure 27.

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The test set ups and computer programs used are very similar for all the device types tested. There are some differences due to the number of ports to be monitored, bias and loading requirements, test equipment availability, and improvements in programming techniques over the term of the contract.

3.3.1 7400 NAND Gate Interference Testing - The 7400 NAND gate contains four 2-input NAND gates in a 14 pin flat pack. Nondestructive measurements were made with the device in active bias states using the RF test fixture described previously. Figure 28 shows the data acquisition and recording set up for interference testing of the 7400. Figures 29 through 33 are block diagrams of the RF portions of the 7400 interference test set ups for each of the five test frequencies. Figure 34 shows the interference test flow diagram for the 7400 device and table 24 is the program for the HP9810A used to incorporate this procedure. To keep track of the data, each device was given a pre-test sample number which encoded all the pertinent data about its test configuration (frequency, port, bias state, and device number from 0 to 9). This sample number is entered into the measurement system manually and becomes a part of each file of data on the magnetic tape.

Table 25 is a listing of the program for the HP9830A to change the data acquired by the HP9810A to an array format, which can be used more efficiently by the HP9830A during later data reduction. Table 26 is a listing of the program for the HP9830A to plot the 7400 data after conversion to the array format.

3.3.2 741 Operational Amplifier Interference Testing - Interference testing on the 741 operational amplifier was conducted in a manner similar to that for the 7400. Figure 35 shows the data acquisition and recording test set up for the testing. Figures 36 through 40 are block diagrams of the RF portions of the test set ups. Table 27 is the program for the HP9810A used to acquire and record the data and table 28 is a list of the data register locations required for the program. The test frequency, port, and device number were encoded and entered into the measurement

system manually. Table 29 is a listing of the program for the HP9830A to change the data acquired by the HP9810A to an array format. Table 30 is a listing of the program for the HP9830A to plot the 741 data.

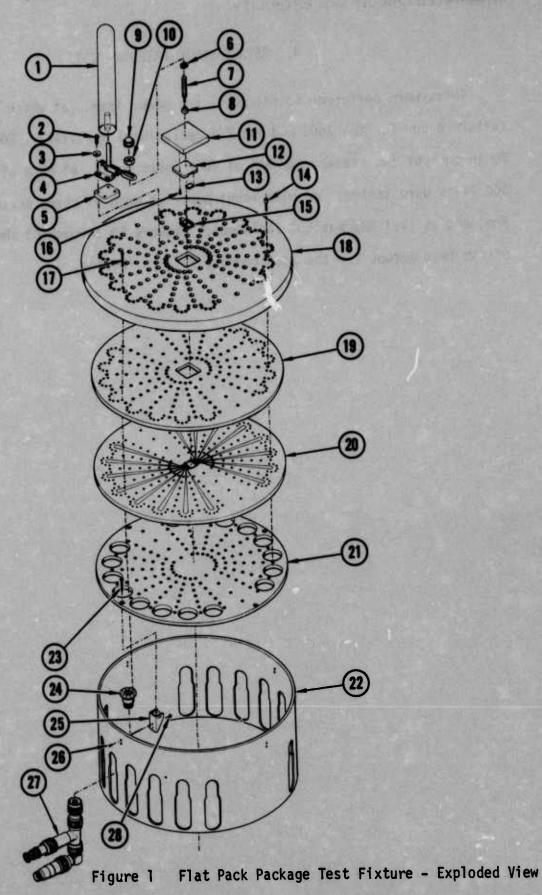
- 3.3.3 MOS 4011 Interference Testing The MOS 4011 contains four 2-input NAND gates utilizing CMOS fabrication techniques in a 14 pin flat pack. Figure 41 shows the data acquisition and recording test set up for interference testing of this device. Figures 42 through 45 are block diagrams of the RF portions of the test set ups. Figure 46 shows the interference test flow diagram and table 31 is the program for the HP9810A used to incorporate this procedure. Table 32 is a list of the data register locations required by the program. The test frequency, port, and device number were encoded and entered into the measurement system manually. Table 33 is a listing of the program for the HP9830A to change the data acquired by the HP9810A to an array format and table 34 is a listing of the program for the HP9830A to plot the MOS 4011 data.
- 3.3.4 2002 Hybrid Interference Testing Figure 47 shows the data acquisition and recording test set up for interference testing of the 2002 hybrid. Figures 48 through 51 are block diagrams of the RF portions of the test set ups. Table 35 is a listing of the program for the HP9810A used for the interference testing and table 36 lists the data register locations required by the programs. Again the test frequency, port, and device numbers were encoded and entered. Table 37 is a listing of the program for the HP9830A to print the 2002 data.
- 3.3.5 Extra Digital Devices Interference Testing The following digital devices received more limited interference testing than the devices discussed above: 3021. 7432, 7402, 7404, 7405, 7450, 7473, and 7479. This testing was performed to verify the MDAC-E 7400 susceptibility model for other devices. These devices were tested using only four input power levels (vs 20 for the others): (1) no input power,
- (2) power which would cause a previously set interference threshold to be crossed.

- (3) maximum power the crystal detectors could safely stand, and (4) a point approximately half-way between the interference threshold and the crystal detector maximum. As shown in figure 52 the interference threshold level was determined using a comparator box, which compared the output from the device under test to a previously determined level. RF power with a pulse width of 500 microsecond was applied to the device when setting up the interference threshold level, to reduce heating effect contributions, but the data was obtained with CW input at that level. Block diagrams of the RF test set ups are the same as for the 2002 (Figures 48 through 51). Table 38 is a listing of the HP9810A program. The data register locations are the same as for the 2002 (table 36). Table 39 is a listing of the program for the HP9830A to reduce the data from the HP9810A.
- 3.4 <u>Special Circuits</u> Design and fabrication of several special circuits were required to bias, load, and test the various types of ICs whose susceptibility was evaluated. These circuits were shown in block diagrams in preceeding paragraphs where applicable. The following paragraphs give a short description of the function of each circuit along with a schematic.
- 3.4.1 <u>Digital Control Box</u> The digital control box supplies worst case loading to the digital device under test while providing voltage and current monitoring of all device terminals. A schematic of the digital control box is shown in figure 53.
- 3.4.2 Operational Amplifier Control Box The operational amplifier control box supplies loading to the operational amplifiers contained in the linear test devices and provides voltage and current monitoring of all device terminals. A schematic of this control box is shown in figure 54.
- 3.4.3 MOS Control Box This circuit provides biasing and loading for the MOS digital devices and also provides for voltage and current monitoring of the devices. The schematic is shown in figure 55.

- 3.4.4 <u>Comparator Box</u> The Comparator Box is used to monitor the output(s) of the devices during the Extra Digital Devices Interference Testing and to indicate when an interference threshold is exceeded. A schematic of the comparator is shown in figure 56.
- 3.4.5 <u>Comparator Control Box</u> The comparator control box supplies loading to the comparator linear test device and provides voltage and current monitoring of all device terminals. A schematic of this control box is shown in figure 57.
- 3.4.6 <u>Voltage Regulator Control Box</u> The voltage regulator control box supplies loading to the positive and negative voltage regulators contained in the linear test devices and provides voltage and current monitoring of all device terminals. A schematic of this control box is shown in figure 58.

#### 4. CATASTROPHIC FAILURE TESTS

Tests were performed to determine the power levels at which catastrophic failure occur for the 7400 and the 741 operational amplifier. 800 7400's were tested: 20 in each of two states, at each of four input ports, at each of five frequencies. 560 741's were tested: 20 with input power at each of seven ports, at each of four frequencies (9.1 GHz was not included). Figures 59 through 63 shows block diagrams of the test setups for the catastrophic failure testing.



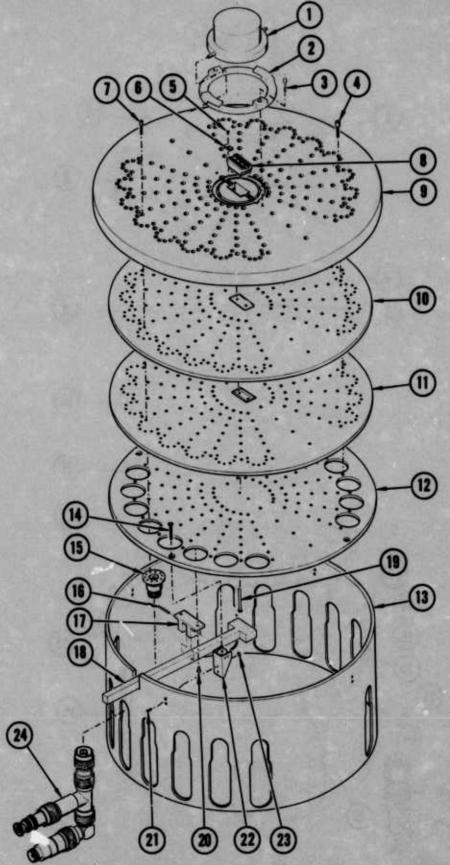
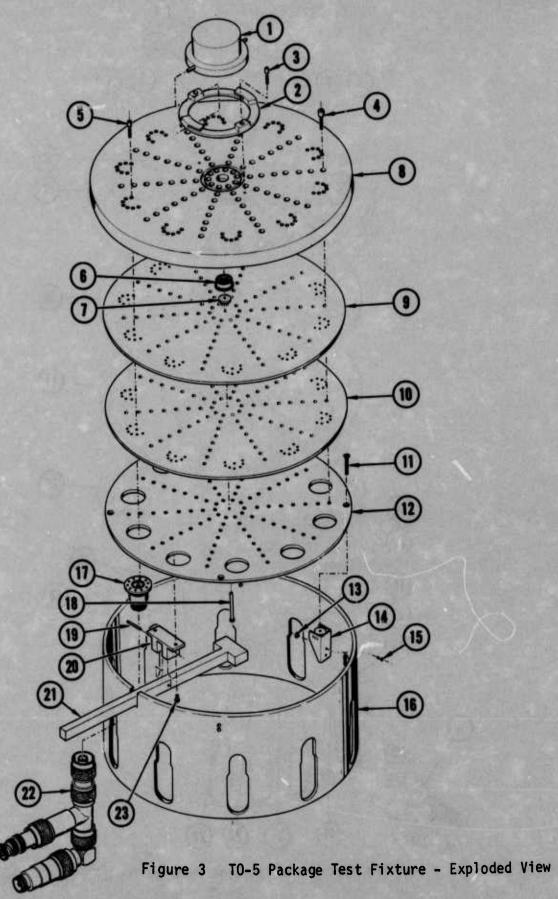


Figure 2 Dual In-Line Package Test Fixture - Exploded View



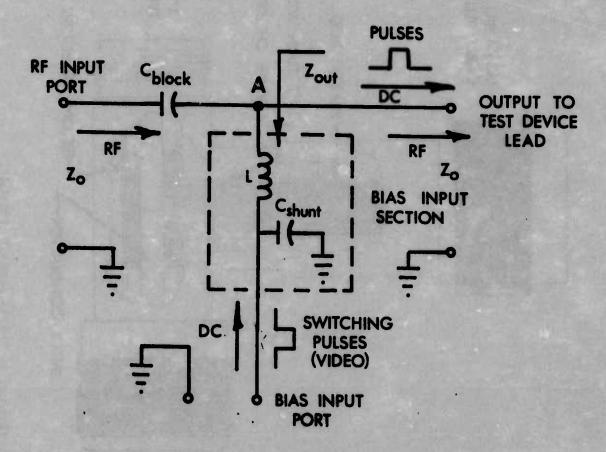


Figure 4 Bias Unit With 2 1/2 Turn Ferrite Choke

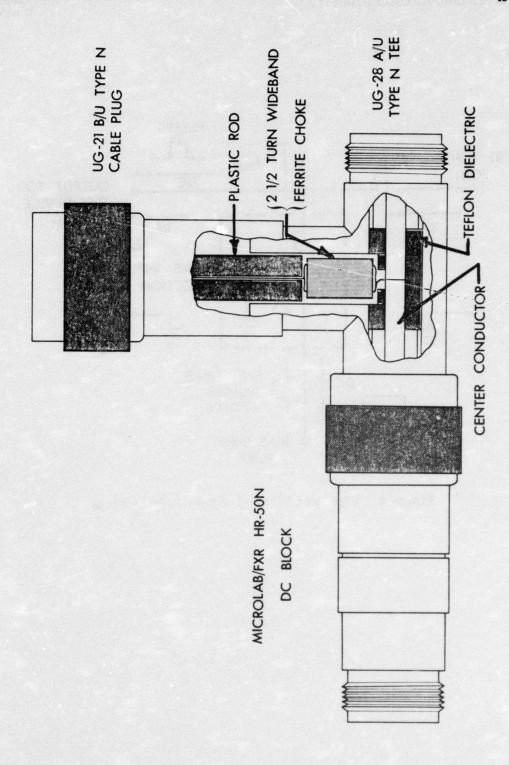
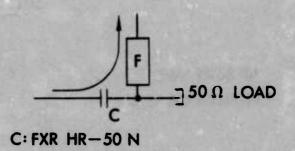


FIGURE 5 CUTAWAY DRAWING OF THE ASSEMBLED BIAS UNIT



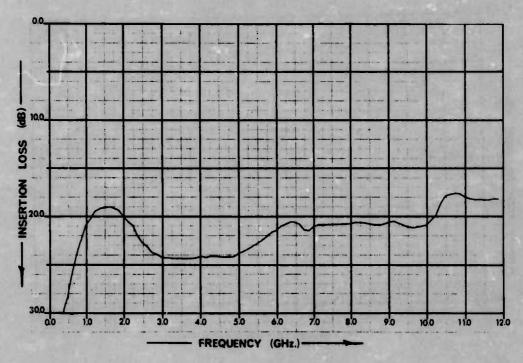


FIGURE 6 RF ISOLATION FROM RF PATH TO BIAS INPUT PORT

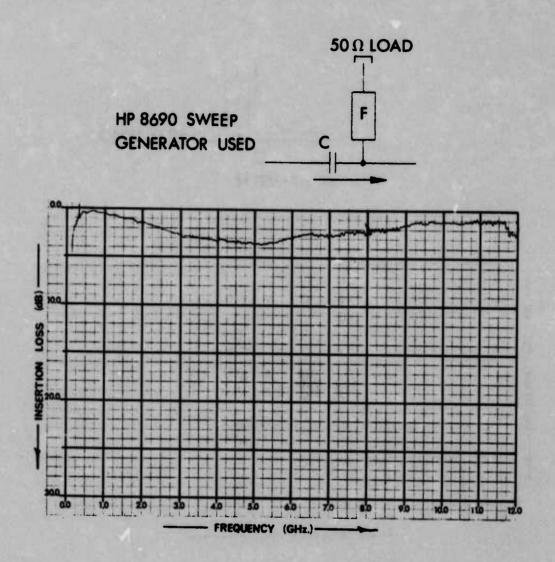


FIGURE 7 BIAS UNIT RF PATH INSERTION LOSS

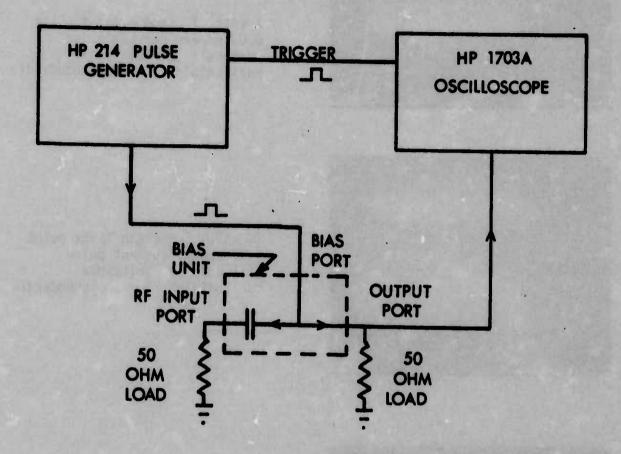
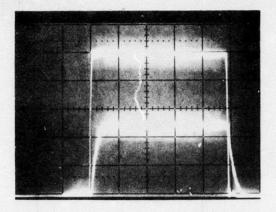
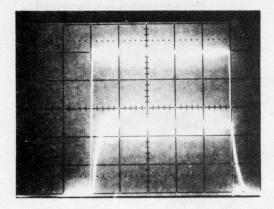


FIGURE 8 SETUP USED TO MEASURE CURRENT SATURATION EFFECTS UPON THE 2 1/2 TURN FERRITE CHOKE

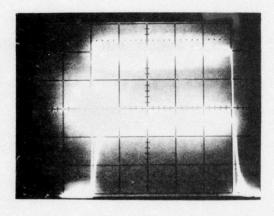


Top pulses in each photograph are input pulses to the bias unit. The bottom pulses are the output pulses from the bias unit's output port. All pulses are delivered to a 25 ohm load.

l volt, l µsecond input pulse 0.01 ampere current pulse vertical: .20 volts/div horizontal: 200 nanoseconds/div

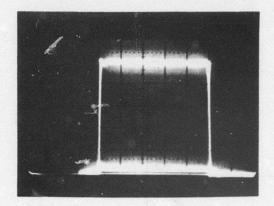


10 volt, 1  $_{\mu}second$  input pulse 0.10 ampere current pulse vertical: 2 volts/div horizontal: 200 nanoseconds/div



100 volt, 1 µsecond input pulse
1.0 ampere current pulse
vertical: 20 volts/div
horizontal: 200 nanoseconds/div.

FIGURE 9 SATURATION EFFECTS FROM HIGH CURRENT LEVELS UPON THE FERRITE CHOKE



Vertical: 2 Volts/div 0.08 amp/div

Horizontal: 200 nanosecond per div.

Upper trace: open circuit voltage available from

generator

Lower trace: voltage delivered to RF generator

FIGURE 10 ISOLATION OF THE RF GENERATOR FROM INPUT PULSES DUE TO THE MICROLAB/FXR DC BLOCKS CAPACITIVE REACTANCE

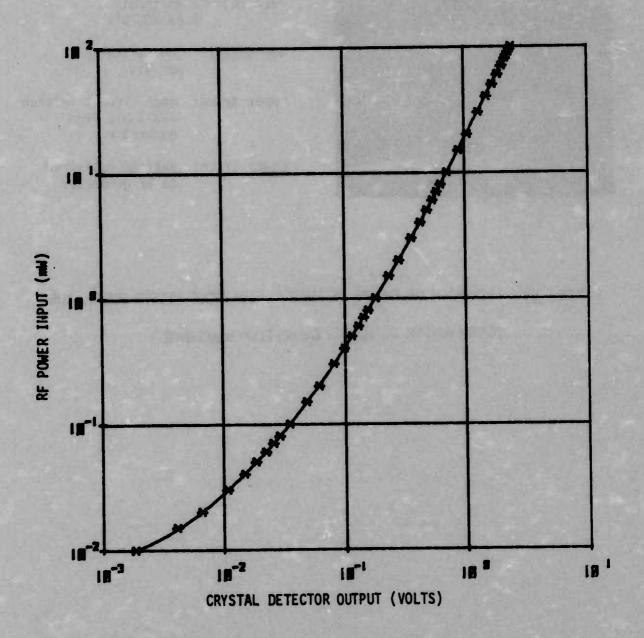


FIGURE 11 TYPICAL CRYSTAL CALIBRATION CURVE

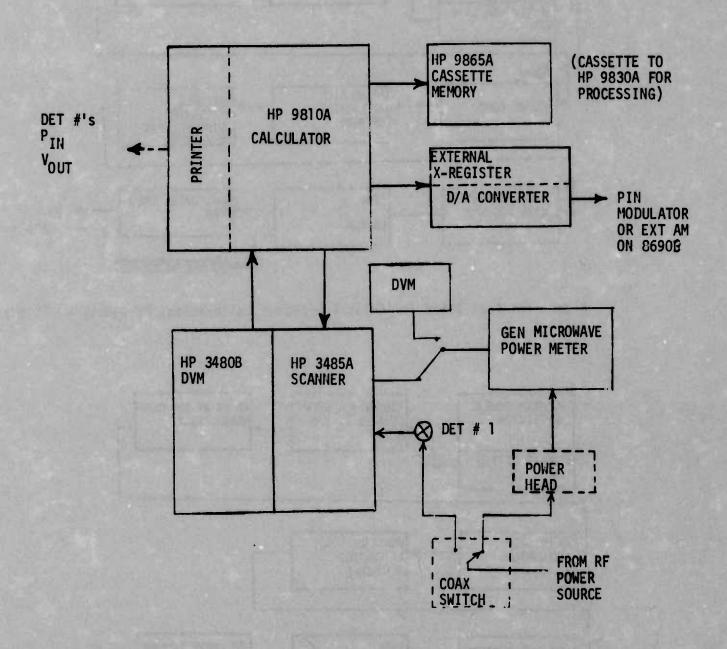


Figure 12 GENERAL TEST SETUP FOR CRYSTAL DETECTOR CALIBRATION

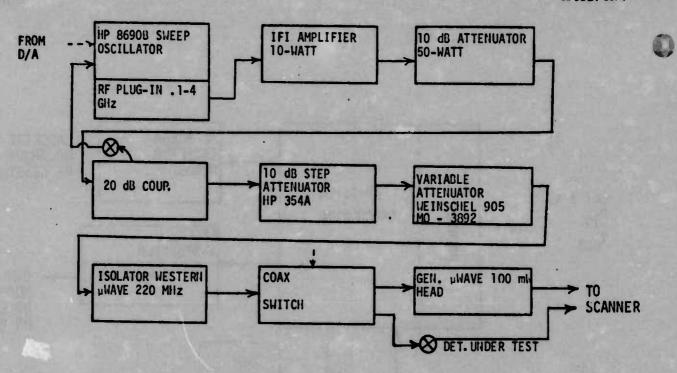


Figure 13 Test Setup for Crystal Detector Calibration, Frequency = .22 GHz

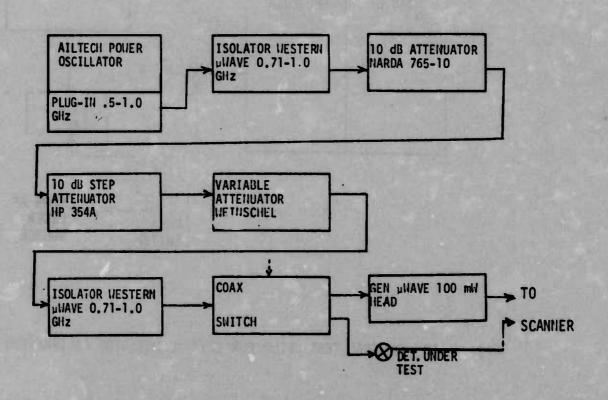


Figure 14 Test Setup for Crystal Detector Calibration, Frequency = 0.91 GHz

A

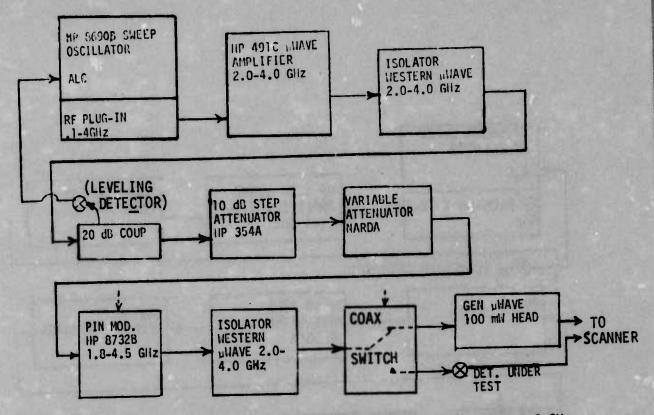


Figure 15 Test Setup for Crystal Detector Calibration, Frequency = 3 GHz

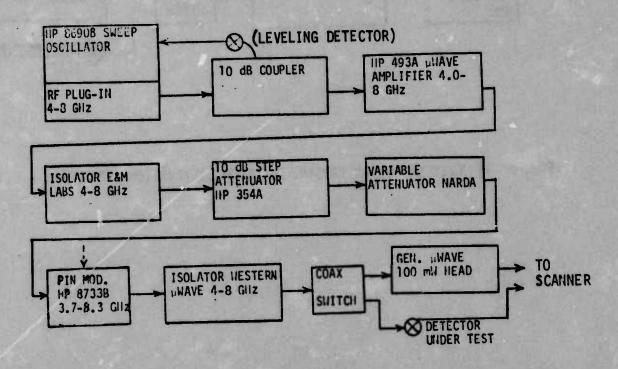


Figure 16 Test Setup for Crystal Detector Calibration, Frequency = 5.6 GHz.

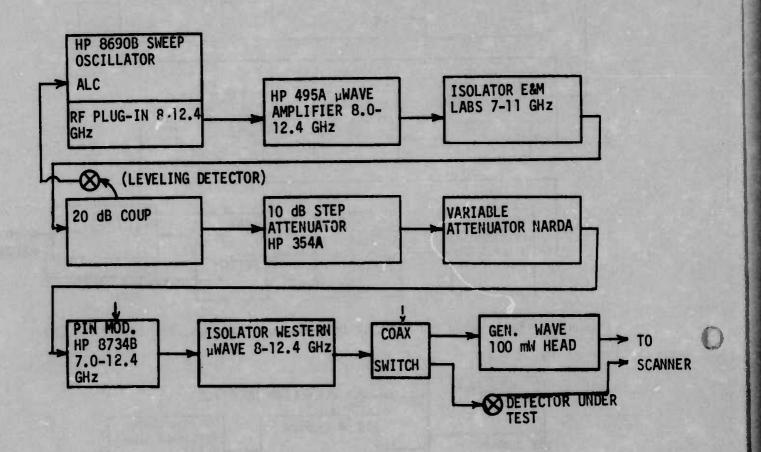
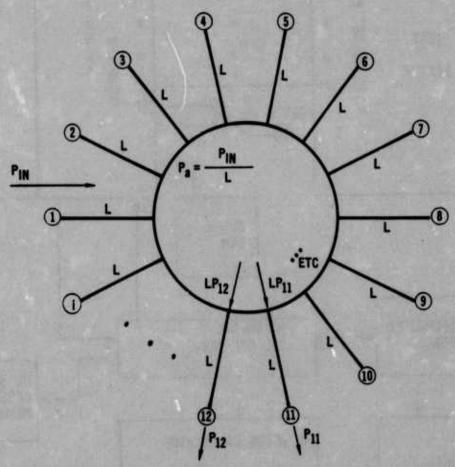


Figure 17 TEST SETUP FOR CRYSTAL DETECTOR CALIBRATION, FREQUENCY = 9.1 GHz



 $P_a$  - POWER AVAILABLE FOR DISTRIBUTION TO OUTPUT PORTS  $P_j$  - POWER MEASURED OUT OF J'TH PORT

$$P_a = \frac{P_{IN}}{L} = \sum_{j=1}^{I} LP_j \text{ HENCE, } L^2 = \frac{P_{IN}}{i}$$

$$\sum_{j=1}^{S} P_j$$

FIGURE 18 DETERMINATION OF FIXTURE DISSIPATION LOSS

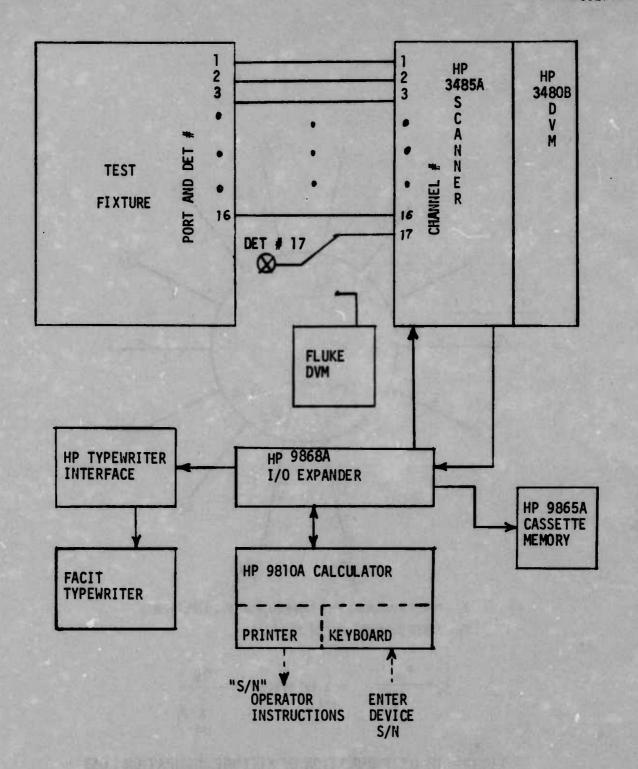


Figure 19 HP 9810A DATA SYSTEM FOR ALL FREQUENCIES FOR FIXTURE CALIBRATION

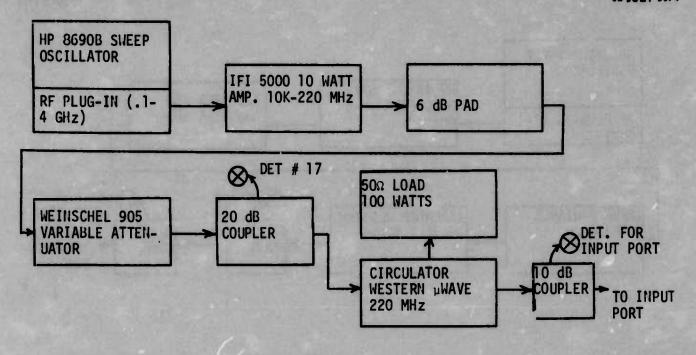


Figure 20 RF SETUP FOR FIXTURE CALIBRATION f = 0.22 GHz

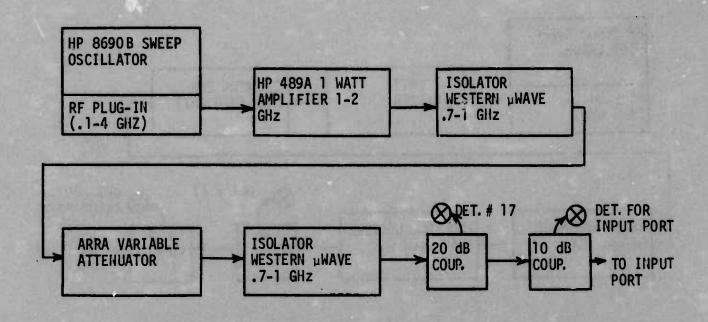


Figure 21 RF SETUP FOR FIXTURE CALIBRATION f = 0.91 GHz

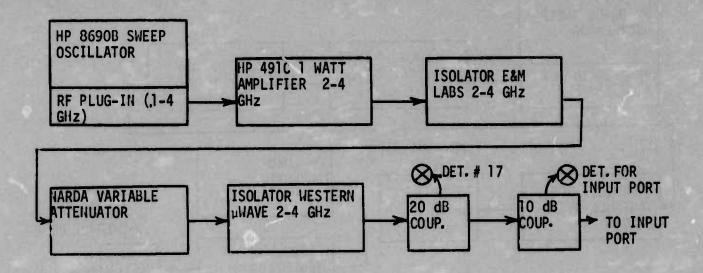


Figure 22 RF SETUP FOR FIXTURE CALIBRATION f = 3.0 GHz

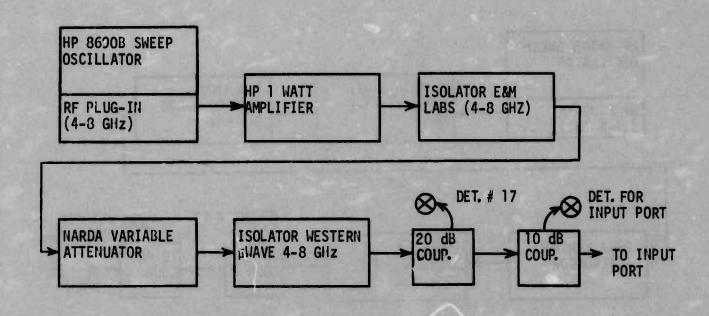


Figure 23 RF SETUP FOR FIXTURE CALIBRATION f = 5.6 GHz

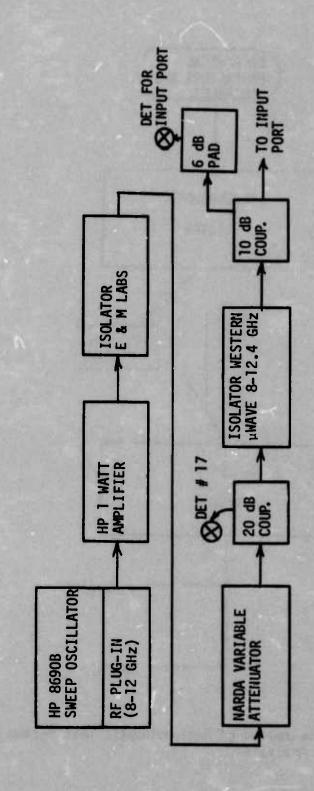


Figure 24 RF SETUP FOR FIXTURE CALIBRATION f = 9.1 GHZ

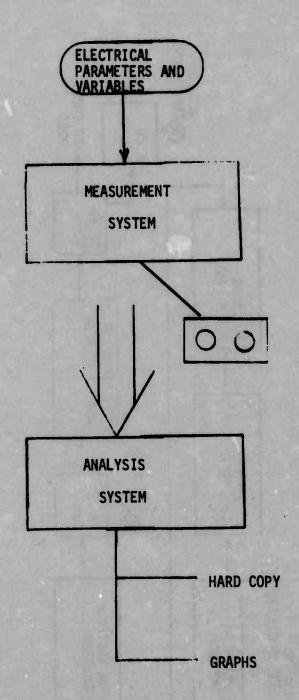
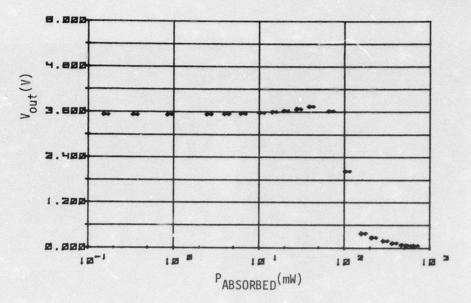


Figure 25 Illustration of Semi-Automatic Test System Measurement and Analysis



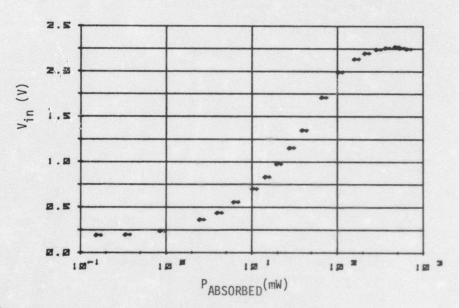


FIGURE 26 EXAMPLES OF V<sub>OUT</sub> AND V<sub>IN</sub> VS P<sub>ABSORBED</sub>, RF INJECTED INTO INPUT PORT OF 7400 DEVICE.

INPUT LOW, OUTPUT HIGH BIAS STATE, 220 MHz



38

A

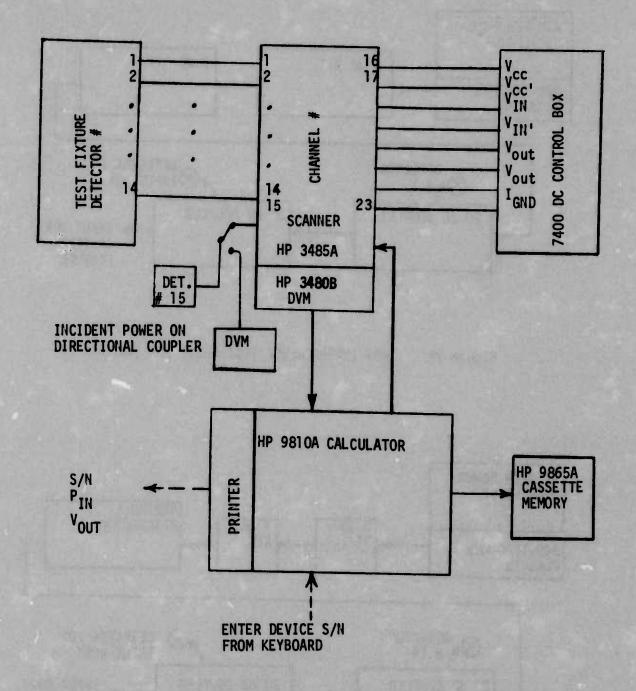


Figure 28 GENERAL TEST SETUP FOR 7400 INTERFERENCE TESTING

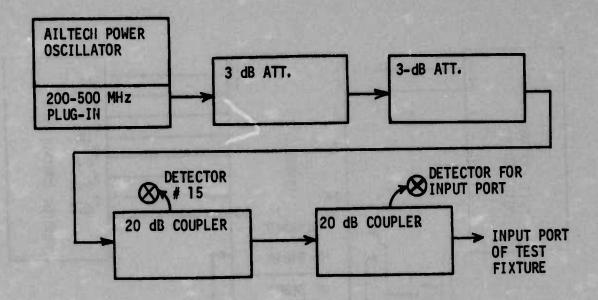


Figure 29 7400 INTERFERENCE TEST SETUP FOR .22 GHz

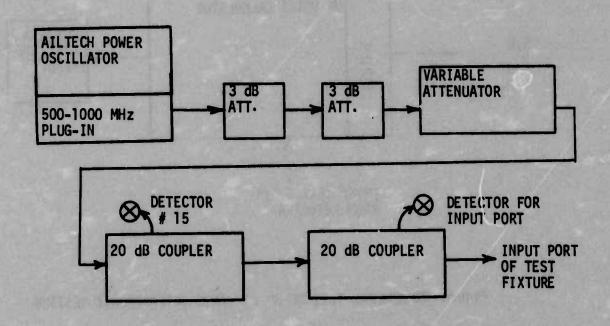


Figure 30 7400 INTERFERENCE TEST SETUP FOR .91 GHz

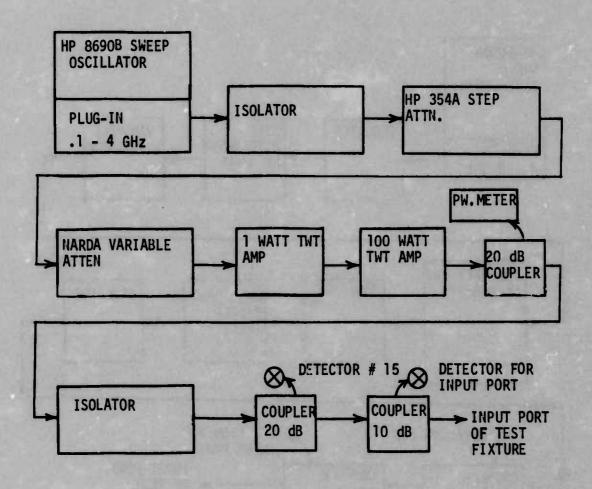


Figure 31 7400 INTERFERENCE TEST SETUP FOR 3.0 GHz

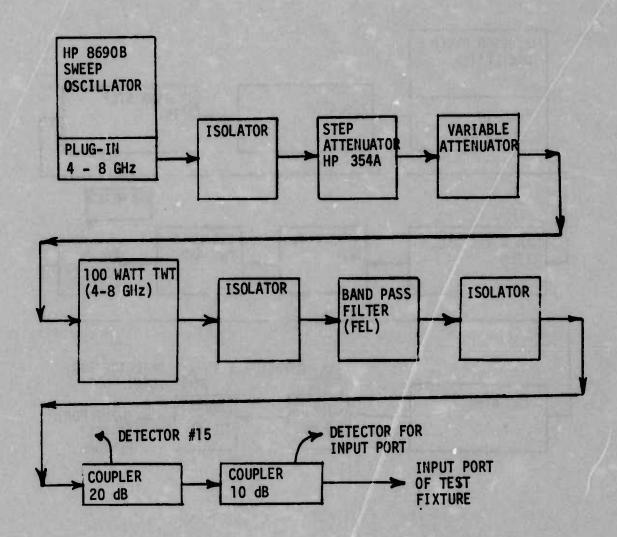
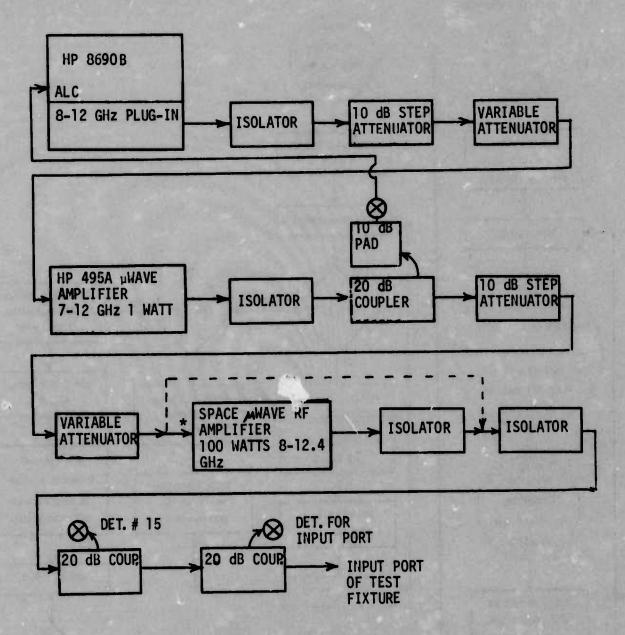


Figure 32 7400 Interference Test Setup for 5.6 GHz



\* USE 100-WART AMPLIFIER AND ISOLATOR COMBINATION ONLY AS NEEDED

Figure 33 7400 INTERFERENCE TEST SEJUP FOR 9.1 GHz

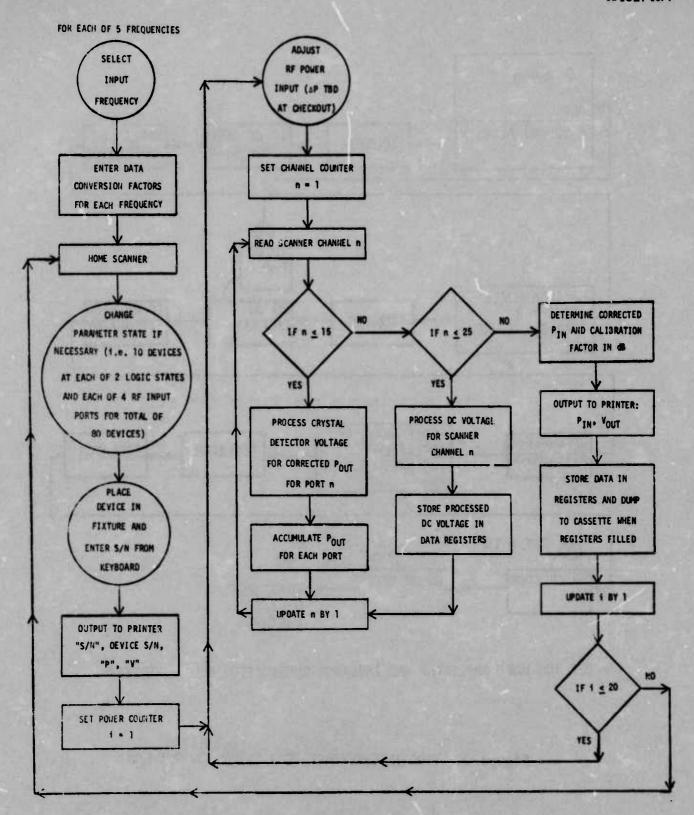


FIGURE 34 7400 INTERFERENCE TEST FLOW DIAGRAM

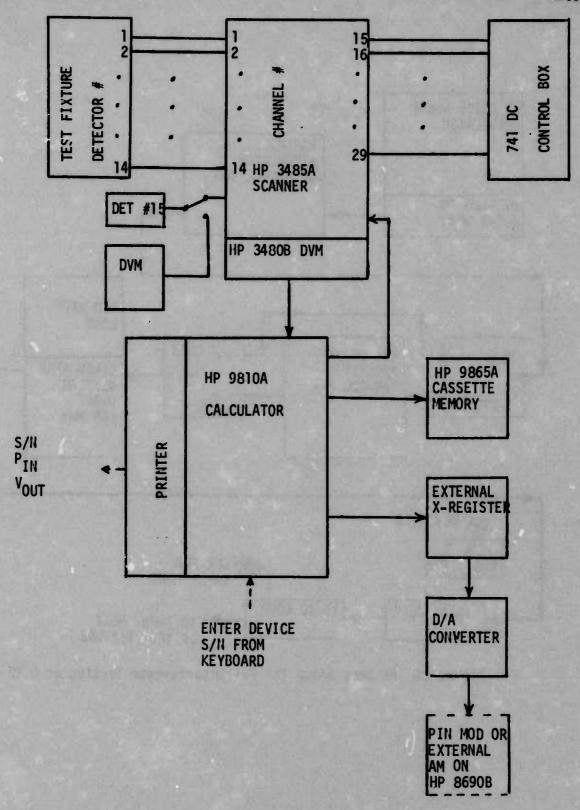


Figure 35 General Test Setup for 741 Interference Testing

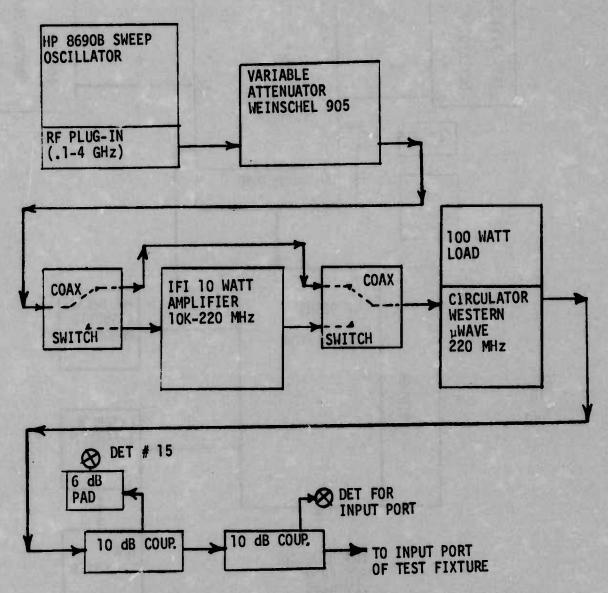


Figure 36 RF Test Setup for 741 Interference Testing at 0.22 GHz

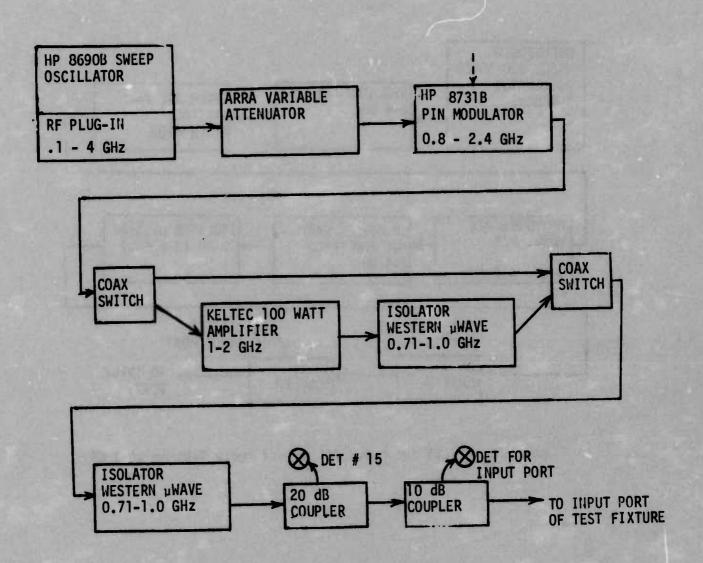


Figure 37 RF Test Setup for 741 Interference Testing at 0.91 GHz

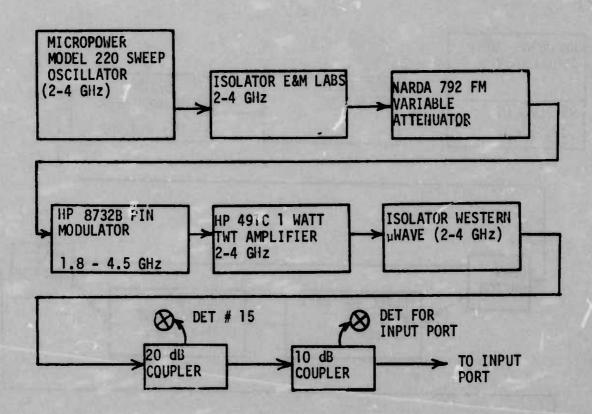


Figure 38 RF Test Setup for 741 Interference Testing at 3 GHz

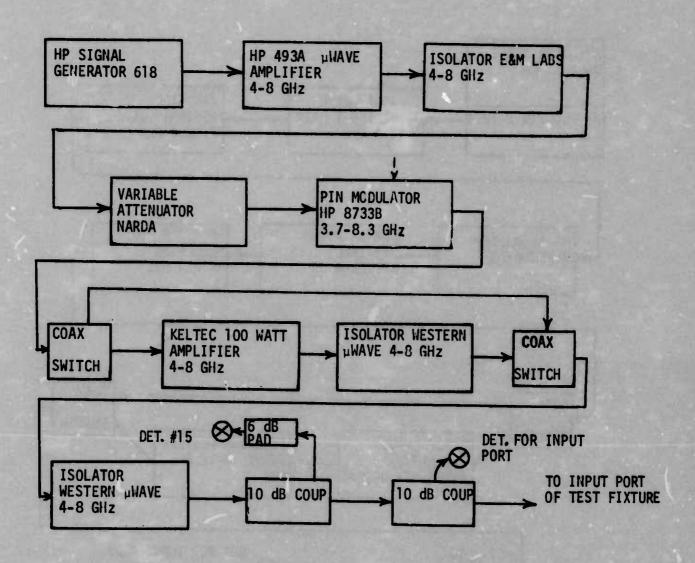


Figure 39 RF Test Setup for 741 Interference Testing at 5.6 GHz

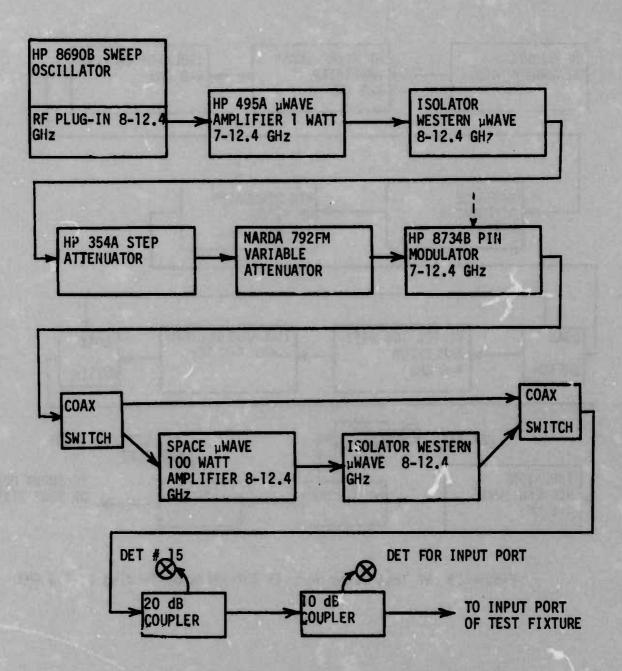


Figure 40 741 Interference Test Setup for f = 9.1 GHz

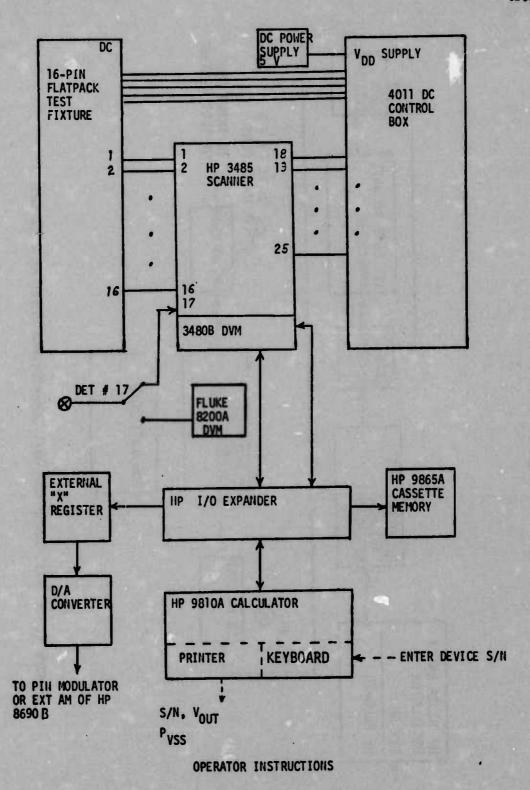


Figure 41 General Test Setup for MOS 4011 Interference Testing

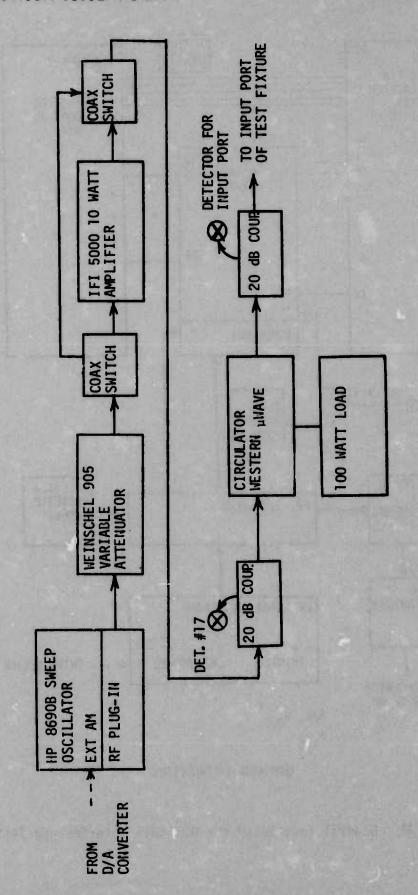


Figure 42 RF Test Setup for 4011 Interference Tests at 0.22 GHz

0

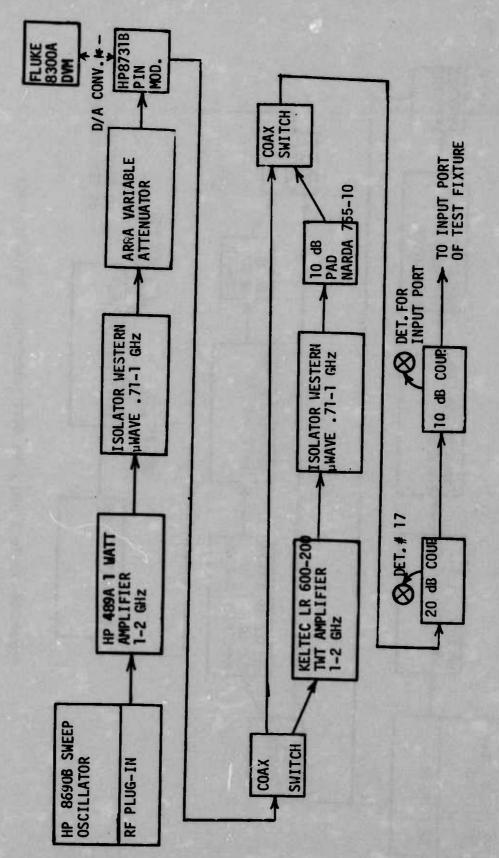


Figure 43 RF Test Setup for 4011 Interference Tests at 0.91 GHz

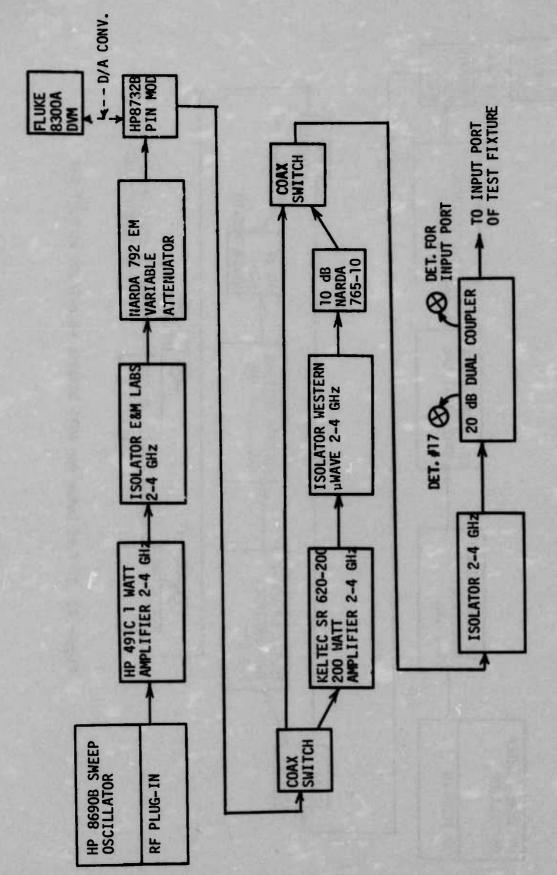


Figure 44 RF Test Setup for 4011 Interference Tests at 3 GHz

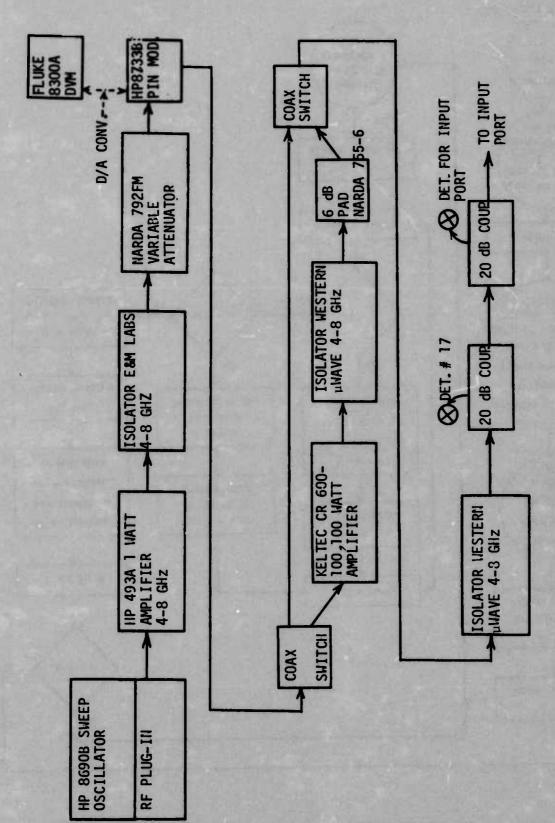


Figure 45 RF Test Setup for 4011 Interference Tests at 5.6 GHz

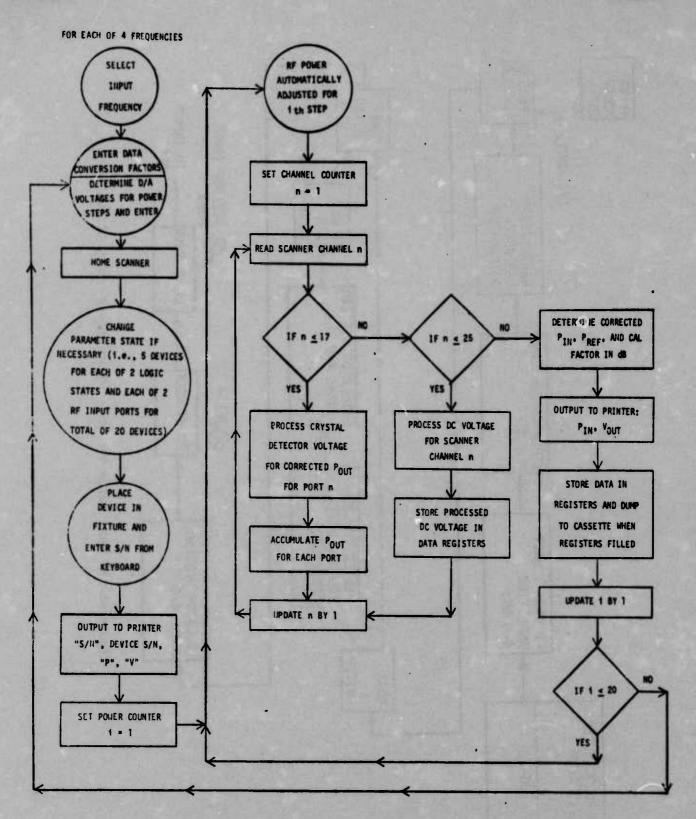


Figure 46 4011 Interference Test Flow Diagram

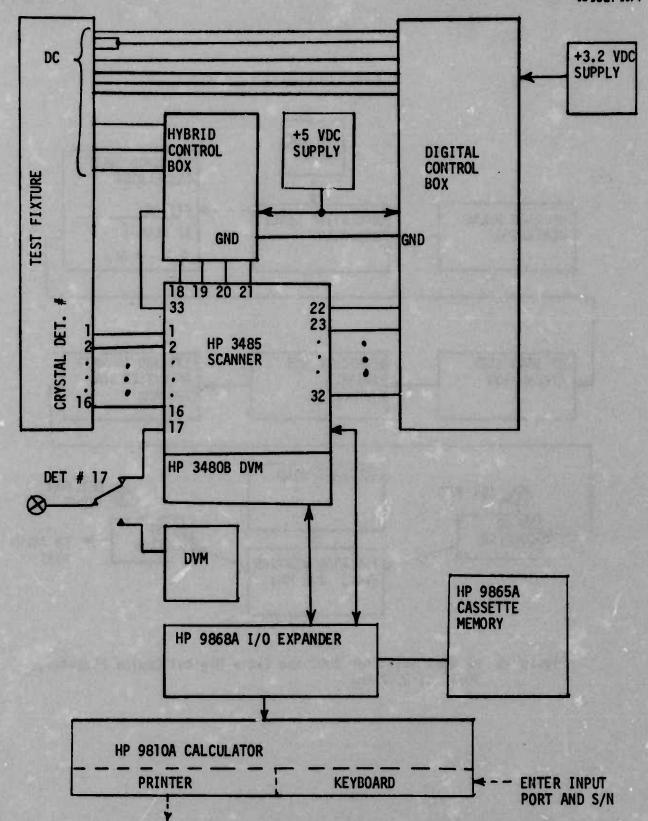


Figure 47 General Test Setup for 2002 Hybrid Interference Test

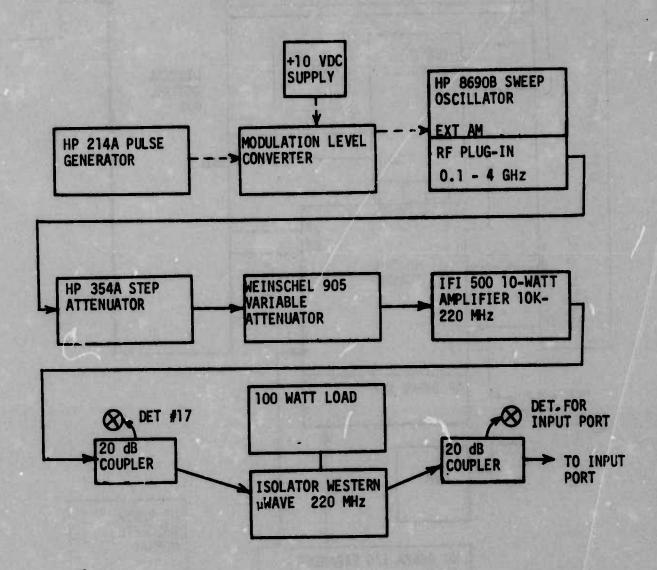
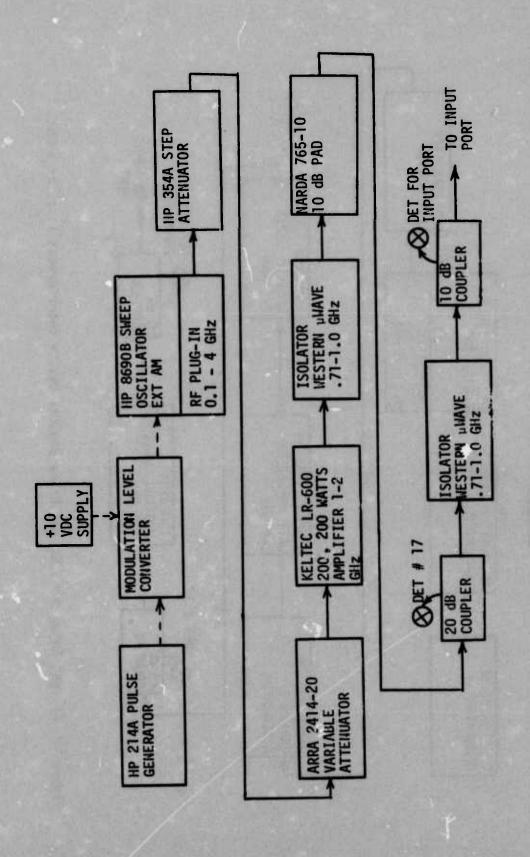
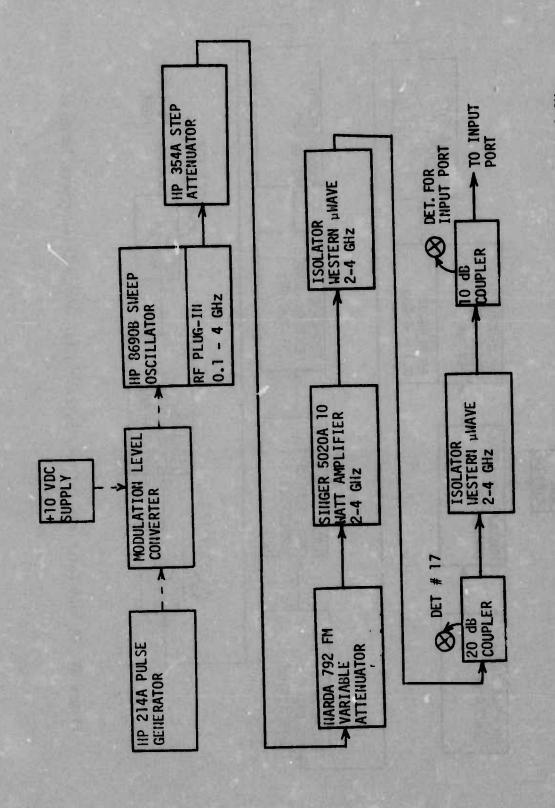


Figure 48 RF Test Setup for 2002 and Extra Digital Device Interference Tests at 0.22 GHz

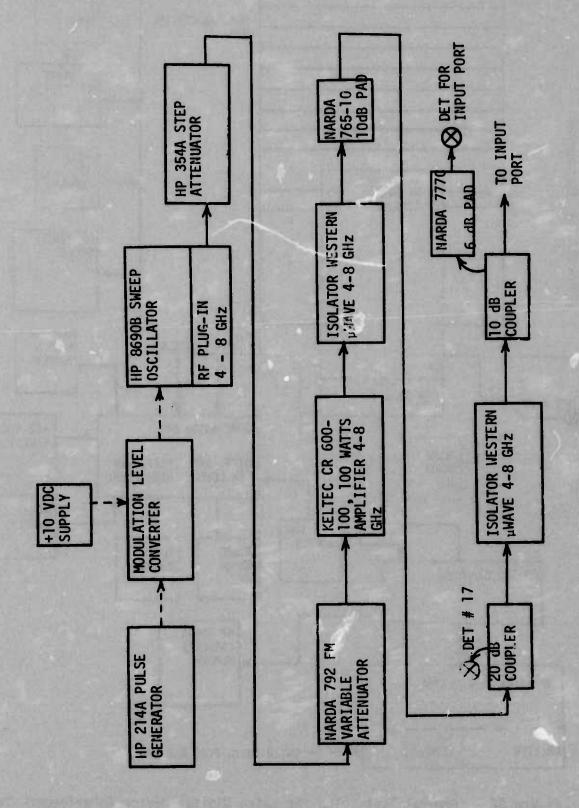


RF Test Setup for 2002 and Extra Digital Device Interference Tests at 0.91 GHz Figure 49



RF Test Setup for 2002 and Extra Digital Device Interference Tests at 3 GHz Figure 50

0



RF Test Setup for 2002 and Extra Digital Device Tests at 5.6 GHz Figure 51

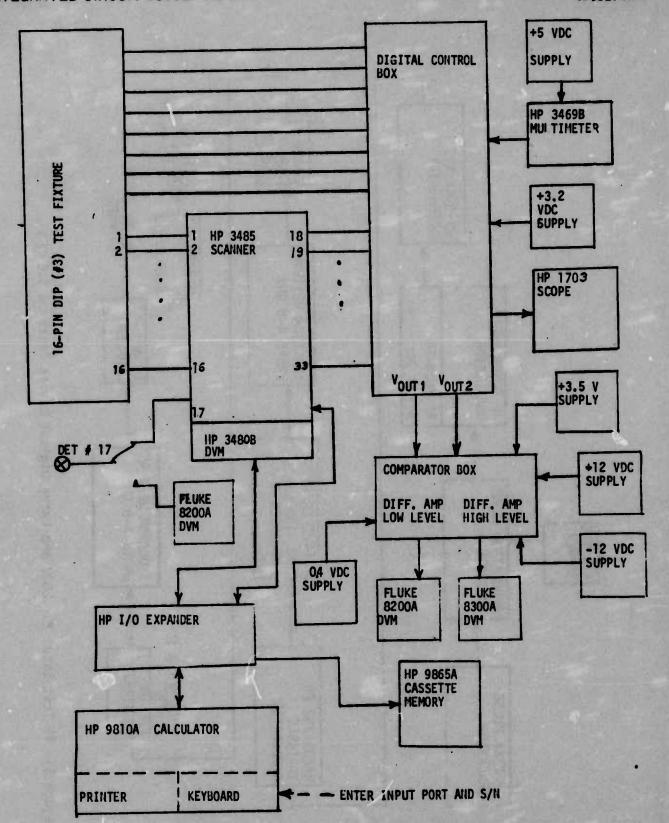
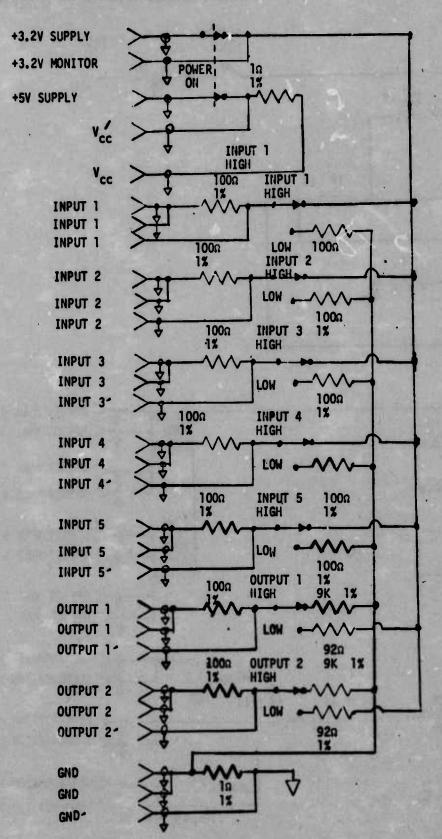


Figure 52 General Test Setup for Extra Digital Device Interference Testing

A



BNC CONNECTOR
ALL SWITCHES
MINIATURE

Figure 53 Schematic: Digital Control Box

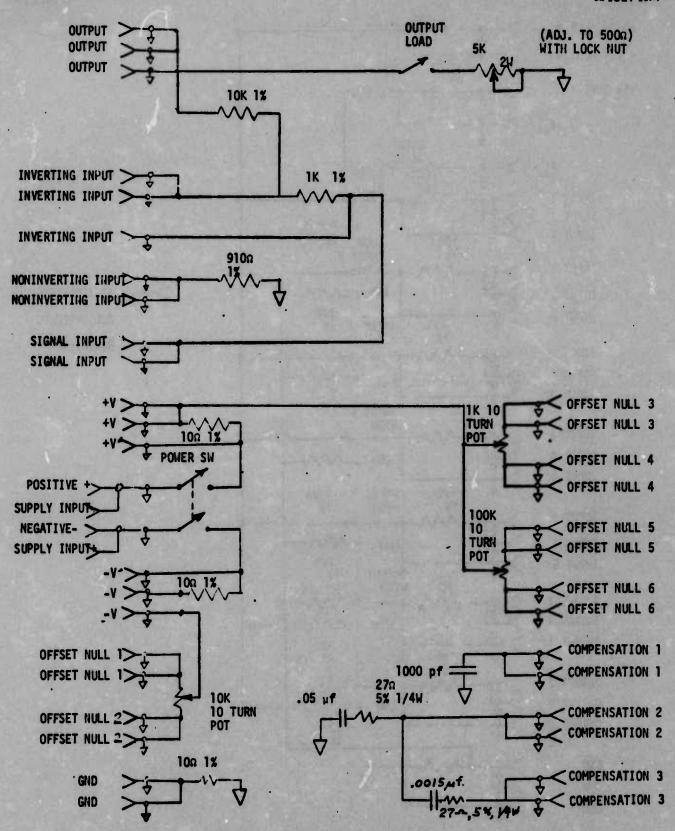


Figure 54 Schematic: Op-Amp Control Box

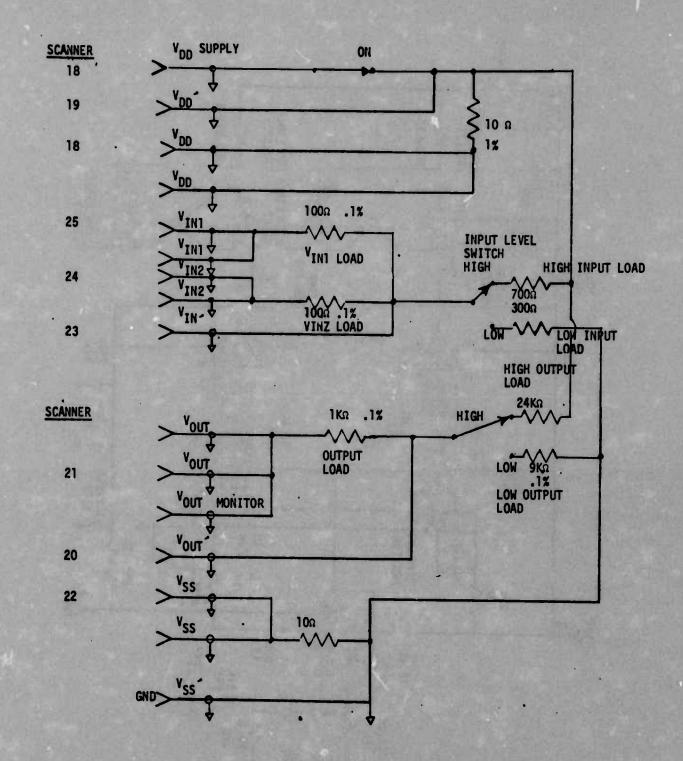


Figure 55 Schematic: MOS Control Box

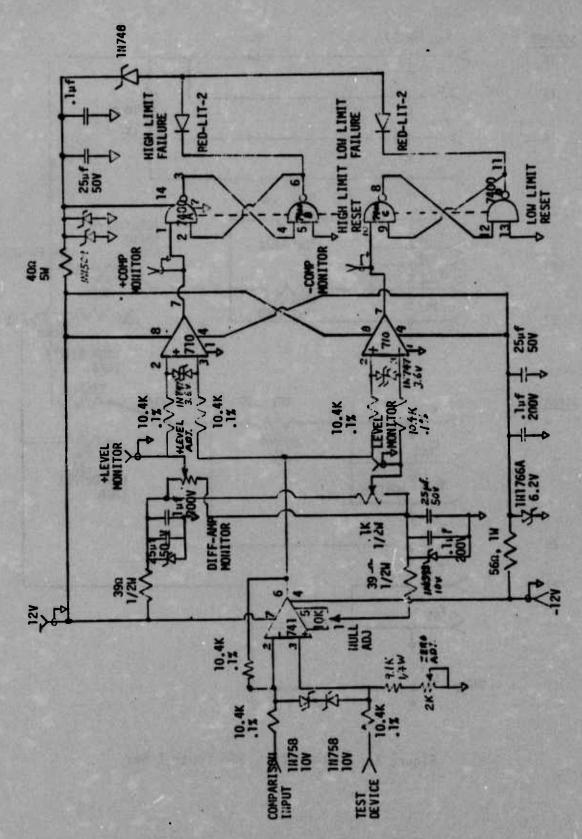


Figure 56 Schematic-Comparator

A

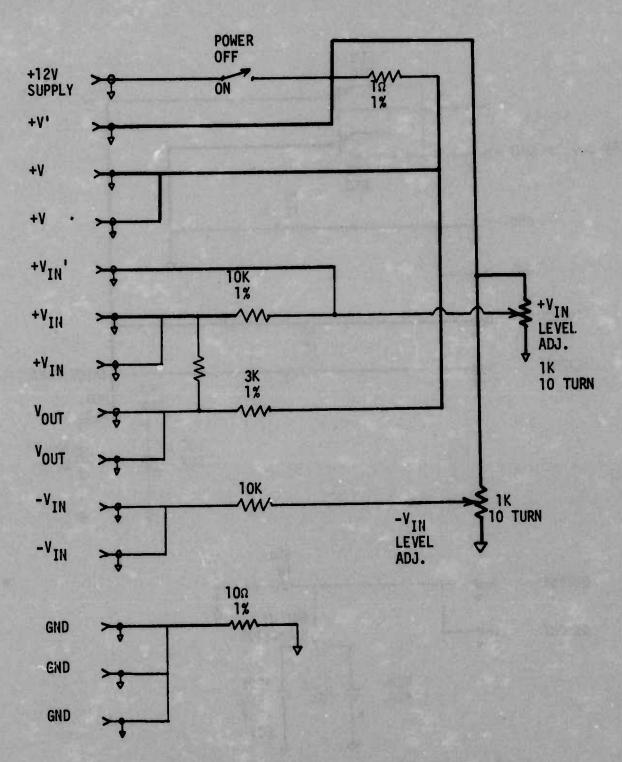


Figure 57 Schematic: Comparator Control Box

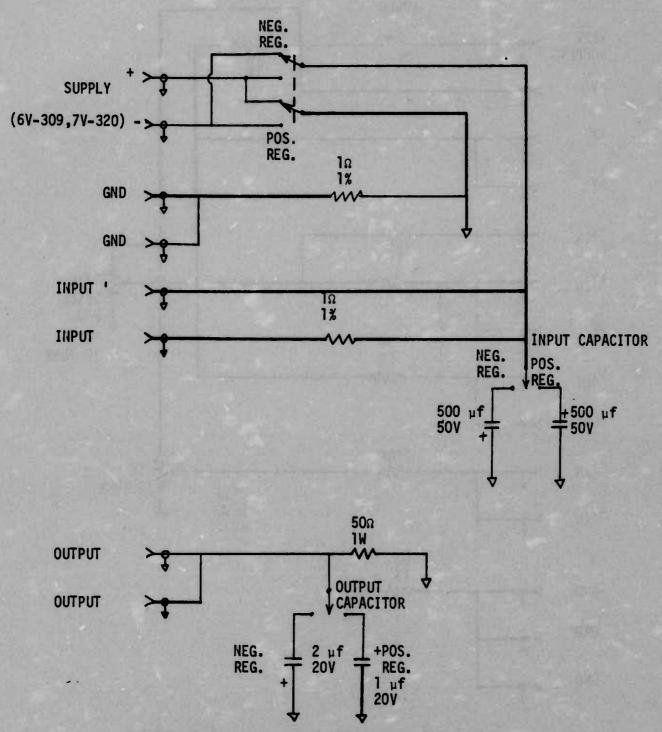


Figure 58 Schematic: Voltage Regulator Control Box

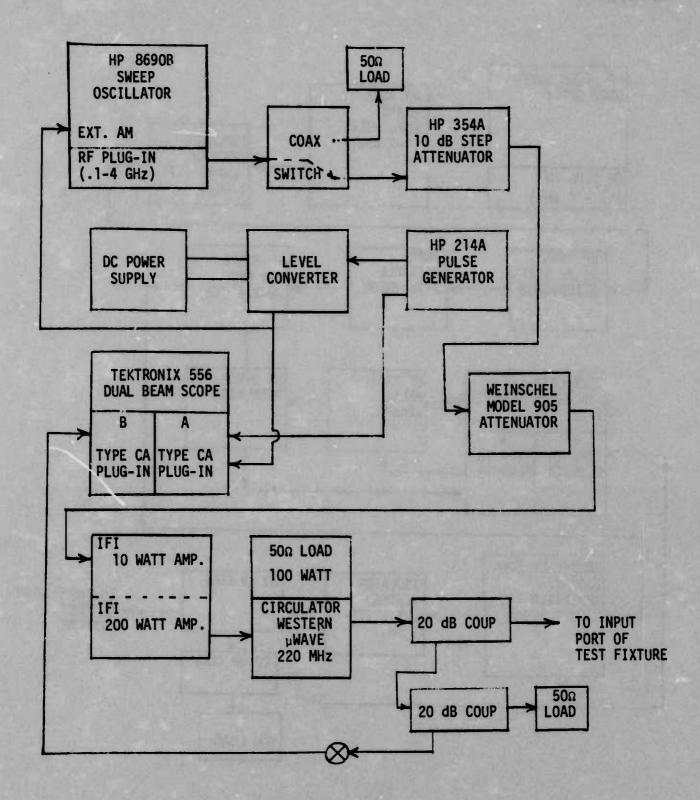


FIGURE 59 TEST SETUP FOR CATASTROPHIC FAILURE TESTING OF 7400 AND 741 AT C.22 GHz

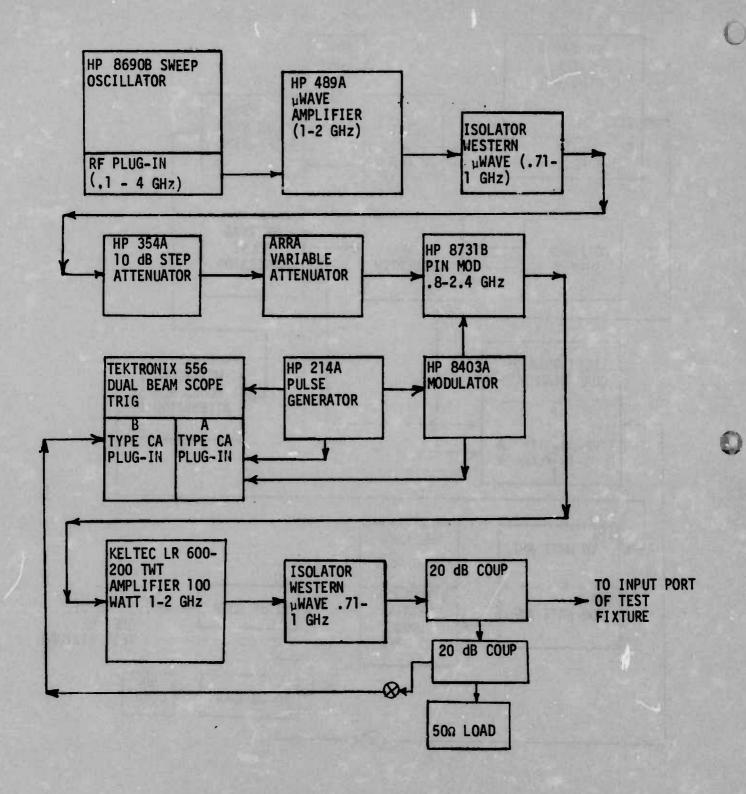


Figure 60 Test Setup for Catastrophic Failure Testing of 7400 and 741 at 0.91 GHz

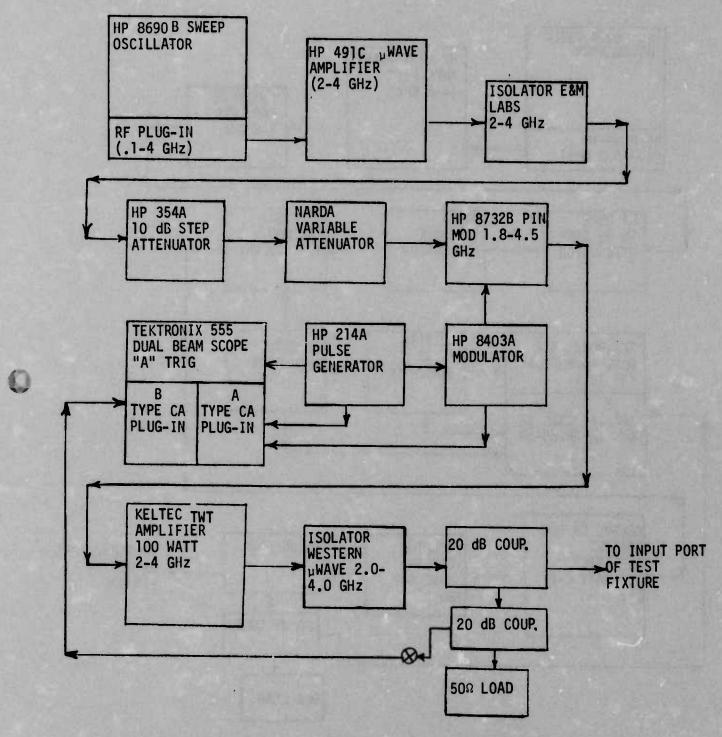


Figure 61 Test Setup for Catastrophic Failure Testing of 7400 and 741 at 3 GHz

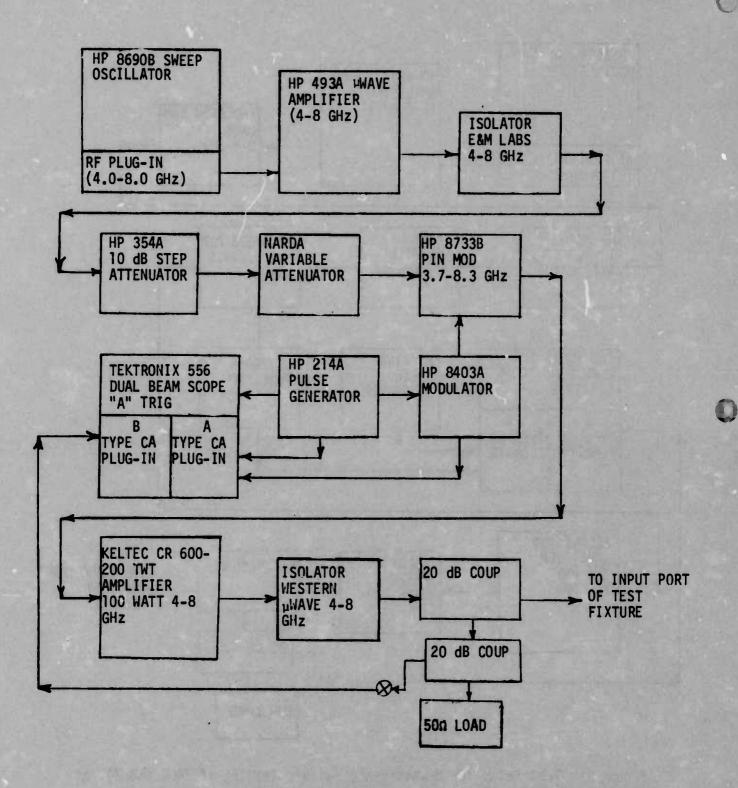


Figure 62 Test Setup for Catastrophic Failure Testing of 7400 and 741 at 5.6 GHz

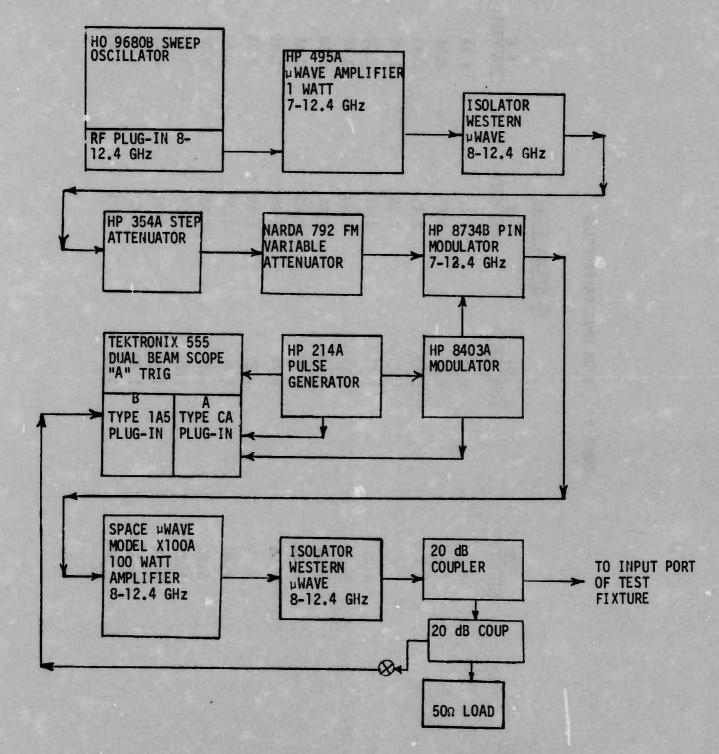


Figure 63 Test Setup for Catastrophic Failure Testing of 7400 9.1 GHz

TABLE 1 BIAS UNIT CALIBRATION

	FREC	FREQUENCY (GHZ)	
.22 L055 (dB)	.91 (ab) \$301	3 LOSS (dB)	
4.00	1.19	2.48	
4.27	1.18	2.51	
4.52	1.14	2.45	
5.02	1.29	2.55	
4.27	1.15	2.71	
5.02	1.25	2.53	
4.34	1.13	2.44	
4.34	1.18	2.63	
5.59	1.28	2.49	
4.70	1,22	2,55	
4.90	1.19	2.30	
4.90	1.23	2.65	
4.30	1.20	2.71	
4.48	1.13	2.34	
4.63	1.13	2.57	
3,94	1,05	2.13	

5.6 -055 (dB) 2.84 2.85 2.85 3.06 3.15 3.08 3.42 2.93 3.28 3.28 3.28 3.28 3.48 3.48

UNIT NO.

2
2
4
4
5
5
7
7
11
12
13
14

### TABLE 2 TYPICAL CRYSTAL CALIBRATION DATA

S/N = 2.91000

#### COEFFICIENTS

B(	0	) =	1.2707600
B( B( B(	1	)=	1.8522600
B(	2	) =	0.1669000
B(	3	)=	-0.0268600

VOLTS 0.00184 0.00410 0.00659	MILLIWATTS 0.01000 0.01500 0.02000	9.01006 0.01464	ERROR(%) -0.63063 2.39674
0.01075	0.03000	0.02011 0.02993 0.04034	-0.56073 0.22854 -0.85928
0.01832 0.02198	0.05000	0.04985	0.30539
	0.06000	0.06039	-0.65043
0.02530 0.02840	0.07000	0.07045	-0.64706 -0.33626
0.03432	0.10000	0.10012	-0.11734
0.04746	0.15000	0.14917	0.55004
0.06032	0.20000	0.20361	-1.80563
0.08012	0.30000	0.29934	0.21924
0.11443	0.50000	0.49805	0.38929
0.13050		0.60501	-0.83448
0.14400	0.70000	0.70156	-0.22314
0.15710	0.80000	0.80105	-0.13118
0.18170	1.00000	1.00314	-0.31351
0.23200	1.50000	1.47753	1.49824
0.28080		2.01529	-0.76460
0.35440	3.00000	2.96917	1.02781
	4.00000	3.97940	0.51500
0.47730	5.00000	4.94206	1.15974
0.53070	6.00000	5.94709	0.88191
0.57730	7.00000	6.89731	1.46695
0.62370	8.00000	7.91132	1.10851
0.70580	10.00000	9.87174	1.28260
0.88600 1.05200 1.29600	15.00000 20.00000 30.00000	14.92309 20.49366	0.51275
1.51000	40.00000	30.29784 40.50085 50.20193	-0.99280 -1.25212 -0.40387
1.86300	60.00000	60.66256	-1.10427
2.00900		70.23142	-0.33060
2.14900	80.00000	80.09138	-0.11423
2.27600	90.00000	89.61976	0.42249
2.38900	100.00000	98.56803	1.43197
2.2000	100.0000	20.70007	1.47131

RMS ERROR = 0.98765 PERCENT

Table 3 Crystal Detector Calibration for .22 GHz

CRYSTAL	B(0)	B(1)	B(2)	B(3)
1	1.21158	1.81590	0.291131	0.0350609
2 3	1.24074	1.79556	0.297538	0.0373098
2	1. 23564	1.81008	0.322782	0.0424489
4	1.20574	1.86404	0.314155	0.0384294
2	1.19481	1.85190	0.197600	0.0000358
6	1.24345	1.83651	0.276008	0.0322073
7	1. 18596	1.85907	0.241479	0.0201003
8	1.20217	1.83820	0.214148	0.0081422
9	1.24621	1.87547	0.226720	0.0109330
10	1.18101	1.88188	0.290815	0.0348513
11	1.26691	1.86180	0.249975	0.0214213
12	1.24609	1.81700	0.256647	0.0257495
13	1.28168	1.87127	0.311244	0.0386666
14	1.26642	1.79186	0.212334	0.0139630
15	1. 25083	1.84017	0.235486	0.0199060
16	1.27627	1.99836	0.345040	0.0421244
17	1.22667	1.79601	0. 235048	
		, , , , , , ,	0. 277040	0.0192368

Table 4 Crystal Detector Calibration Coefficients for .91 GHz

CRYSTAL	B(0)	B(1)	B(2)	B(3)
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16	1.26608 1.27636 1.28785 1.25658 1.19111 1.23989 1.18055 1.22359 1.24661 1.17248 1.28972 1.24014 1.27212 1.27301 1.24890 1.26884	1.80527 1.77042 1.76456 1.83276 1.84995 1.82310 1.85284 1.83593 1.86559 1.87113 1.84059 1.82607 1.85121 1.79602 1.83210 1.96376	0.259396 0.239902 0.284451 0.261251 0.195178 0.261538 0.233946 0.194614 0.219143 0.280579 0.234094 0.276245 0.295265 0.249553 0.220251 0.302778	0.0271789 0.0204803 0.0353526 0.0262011 0.0018103 0.0256129 0.0147341 0.0014644 0.0094050 0.0299600 0.0162157 0.0304371 0.0335471 0.0256183 0.0115535 0.0292455
17	1.22657	1.80361	0.254249	0.0250931

Table 5 Crystal Detector Calibration Coefficients for 3 GHz

CRYSTAL	B(0)	B(1)	B(2)	B(3)
1	1.27763	1.81892	0.263690	0.0251775 0.0248788 0.0334609 0.0244254 0.0000000 0.0270827 0.0131825 0.0012353 0.0126360 0.0272287 0.0130534 0.0261232 0.0421188 0.0200216 0.0098869 0.0270774 0.03333236
2	1.28302	1.78576	0.253112	
3	1.29163	1.77227	0.280223	
4	1.26470	1.84092	0.261317	
5	1.19930	1.86181	0.198932	
6	1.23358	1.83813	0.272475	
7	1.18078	1.86341	0.238082	
8	1.21794	1.84851	0.202025	
9	1.24672	1.88003	0.233851	
10	1.17681	1.88742	0.284124	
11	1.26364	1.85084	0.233118	
12	1.23927	1.83673	0.272627	
13	1.26724	1.88329	0.329327	
14	1.27187	1.78476	0.251192	
15	1.24135	1.84327	0.223890	
16	1.27151	1.98515	0.307480	
17	1.21854	1.81764	0.280198	

Table 6 Crystal Detector Calibration Coefficients for 5.6 GHz

2       1.28414       1.77989       0.242594       0.020995         3       1.29507       1.77151       0.274308       0.031738         4       1.27982       1.84971       0.265698       0.026129         5       1.22245       1.85525       0.188531       0.000000         6       1.23468       1.83720       0.262285       0.024140         7       1.19720       1.86466       0.229990       0.013057         8       1.22201       1.84760       0.190717       0.000050         9       1.24856       1.88552       0.227181       0.010040         10       1.18795       1.88286       0.278124       0.029521         11       1.27018       1.85684       0.236416       0.018478         12       1.24434       1.84279       0.273079       0.029007         13       1.27030       1.89418       0.329192       0.042646         14       1.26289       1.78335       0.263753       0.027288         15       1.24186       1.84348       0.214324       0.008773	CRYSTAL	B(0)	B(1)	B(2)	3(3)
	3 4 5 6 7 8 9 10 11 12 13 14 15 16	1.28414 1.29507 1.27982 1.22245 1.23468 1.19720 1.22201 1.24856 1.18795 1.27018 1.24434 1.27030 1.26289 1.24186 1.27460	1.77989 1.77151 1.84971 1.85525 1.83720 1.86466 1.84760 1.88552 1.88286 1.85684 1.84279 1.89418 1.78335 1.84348 2.00459	0.242594 0.274308 0.265698 0.188531 0.262285 0.229990 0.190717 0.227181 0.278124 0.236416 0.273079 0.329192 0.263753 0.214324 0.316760	0.0153620 0.0209931 0.0317339 0.0261293 0.0000001 0.0241400 0.0130577 0.0000501 0.0100407 0.0295213 0.0184783 0.0290070 0.0426467 0.0272889 0.0087737 0.0334410 0.0260548

Table 7 Crystal Detector Calibration Coefficients for 9.1 GHz

1 1.32402 1.82107 0.241207 0.0190 2 1.30934 1.80303 0.257192 0.0243 3 1.31229 1.79759 0.285859 0.0328	
4       1.32 211       1.84600       0.239467       0.0163         5       1.28484       1.89469       0.209176       0.0000         6       1.25896       1.86727       0.278290       0.0262         7       1.24194       1.88356       0.236714       0.0142         8       1.23284       1.87247       0.202222       0.0006         9       1.26049       1.90474       0.230906       0.0067         10       1.22897       1.90423       0.271844       0.0235         11       1.30727       1.86117       0.210239       0.0034         12       1.27749       1.83829       0.236720       0.0124         13       1.28878       1.90109       0.308784       0.0347	3200 3895 0000 2121 2114 0000 1021 5726 4527 4962
14 1.25911 1.79075 0.287093 0.034	7386
15 1.24244 1.84655 0.200972 0.0046 16 1.30114 2.05071 0.353879 0.0426 17 1.22237 1.82678 0.288599 0.033	5360

## Table 8 HP 9810A Program for Crystal Detector Calibration

	TADIE O HP 981UA	Program ter Crystal	Detector Calibration
1 1 1 1 1	20		
THE STATE OF	55	0051 - 540	016! -8 044
nuggCL	W 17	0052 IND31	
11 03 [			0102 - LBL51
		0053 I65	0103 E60
HUMAN- F	62	0054XT023	0104CNT47
maggp		9055 C61	0105XEY30
HERE - FR	TT42	0056 H74	
41197 I			0106 303
nces E		0057 34	0107 101
		0058 M70	0108KLY36
H909XT		0059 E60	0109
1:010 ,	seed 5001 cont. 1 1	0060	0110GTO44
111111	IT 17	0061 E60	0111LBL51
11011261			
0013 FM		0062013	0112 C61
		0063FMT42	0113CNT47
1111 d = 5T		0064 1 01	0114 DN25
U015XT	<u> </u>	0065 000	0115 [61
[] [] [ ] [ [ ] [ ] [ ] [ ] [ ] [ ] [ ]	1 йй	0066 UP27	0116 000
0617PH			
111718		0067 614	0117 008
		0068X>Y53	0118 X36
		0069GTO44	9119GTO44
11.20-0		0070S/R77	0120LBL51
U021XT	023	0071LBL51	0121 D63
ПП22 Ь		9072 F 16	
0023LB			0122LBL51
		0073STP41	0123 C61
บค24 B		0074FMT42	0124 UN20
00-25FM		0075 4 64	0125 1 01
0026 4	04	0076 i 0;	0126 000
HA27 1	G 1	0077FMT42	
unigh Fig			0127 1136
11129SF		0078 101	0128GTO44
		0079FMT42	0129LBL51
U030FM		0080PSE57	0130 D63
11121	1747	0081PSE5,	0131L8L51
111132 5	· · · · · · · · · · · · · · · · · · ·	0082FMT42	0133 E69
- HU33 Ø		The state of the s	
11034 Ŭ		0083 3 93	0133XEY30
		0084 3 03	0134 1 BY
##35 o.		008521	0135 0 0e
10036 +		0086 UP27	0136XEY30
- WH37YT	046	0087CNT47	0137X>Y53
UH38 5		0088CNT47	
nu39 ø			0138 DN25
	** **	0089FMT42	0139GTO44
XF		0090 4 04	0140181
0041IN	D31	0091 1 01	0141 D63
11942 5	95	8692FM142	0142 DN25
មាស្ម្រាន ធ្វី		0093 101	
POHÁ FI			014321
		0094FMT42	0144 101
11045 4		0095 UP27	0145 836
иг.46 2		0096 202	0146LBL51
H947XT		0097 101	0147 D63
8648CN		0098 UP27	
0049FR			0148 G15
		009913	0149FEX26
0050FM	1 4 2	010052	0150 ; 03

--04 --27 --00 --42 --05 --23 --44 --51

## Table 8 HP 9810A Program for Crystal Detector Calibration (Cont)

015136	0201 36	<b>M</b> .
	020a DI25	025
0152 Dh 25	0203XEY30	n253 0
0153INT64		
0154XTO23	0204FMT42	0254FMT
0155IND31	0205FMT <u>4</u> 2	11255 5
Ottober or mento	92 <b>96 1</b> 56	0256XT0
0157CNT47	0207XKY52	U257GTO
11158CHT47	0208 M70	0258LBL
0159FNT42	0209IND31	∂259 A
0160FMT42	021073E57	9268LBL
0161YT040	0211CLR20	6261 F
0162IND31	0212INT64	0262FHT
M163 I65	0213X4Y53	√ 0263FMT
	0214INT64	<b>#264</b> 0
9164WT023	0215 0 71	9265 H
0165 C <u>6</u> 1		
0166 H74	0216 L72	9266 H
016734	0217XTO23	0267
0168 D63	0218YT040	The first of the second of the second
0169 E60	0219PSE57	0269 E
0170XTQ23	8220FPT4:	0270CHT
1917121	0221FMT45	0271 o
11172	0222XEY30	0272 A
0173STP41	0223PNT45	0273 N
11:74FMT42	0224 101	0274 G
9175 3 93	0225 UP27	0275 E
	0226 E60	0276FMT
0176 303	0227 404	0277 1
017721	0228 101	0278X10
0178 UP27	0229 UP27	
(1)79 G15		0279 b
11180 1 01	0230 a13	02808/R
0)81 000	0231X <u>Y</u> 58	0281EHD-
₩182DIV35	0232GTO <u>4</u> 4	
0:83YT040	0233LBL51	
4184IND31	0234 B <b>-</b> 66	
11185 +33	0235CHT47	
ŭi86 α13	0235FMI	
0)87XFR67	0237 505	
0188IND31	0238EEX26	
0189 013	0239FMT42	
910277 W 19	0240FMT42	
#190 UP27	0241 a	
0191INT64	0242 6 60	
019234	0242 - 61	
u193 UP27	0243 C61	
u194EEX26	0244 071	
0195 303	0245 <u>0</u> 13	
0196DIV35	0246 <u>1</u> 163	
0197RUP22	0247IFG43	
9198XEY30	0248FMT42	
0199 - 101	0249TP41	
6200 0 - <b></b> 00	0250- 0 10	
5750		

#### Table 9 HP 9830A Program to Convert Data to Matrix Format for 1 Crystal

```
10 DISP "FIRST FILE #":
20 REM PROGRAM TO CONVERT FROM DATA TO MATRIX FORMAT FOR 1 CRYSTAL
30 INPUT N
40 DISP "FIRST MATRIX FILE#";
50 INPUT M
60 DIM A[84,1], CS[8,41]
70 REDIM A[84,1]
80 LOAD DATA N.A
90 C[1,1]=C[2,1]=A[1,1]
100 GOTO 180
110 C[5,1]=C[6,1]=A[43,1]
120 C[7,1]=C[8,1]=A[64,1]
130 GOTO 160
140 IF A[22,1]#C[1,1] THEN 560
150 IF A[1,1]#C[3,1] THEN 560
160 IF I=1 THEN 260
170 FOR J=0 TO 1
180 FOR K=2 TO 41
190 V=A[K,1]
200 P=INT(V)/1000
210 V=10*(V-INT(V))
220 C[1,K]=P
230 C[2,K]=V
240 NEXT K
250 GOTO 400
260 FOR J=0 TO 1
 270 FOR K=2 TO 21
280 V=A[J*21+K,1]
290 P=INT(V)/1000
300 V=10*(V-INT(V))
310 IF J>0 THEN 350
 320 C[ 2*J+3.K]=P
 330 C[2*J+4.K]=V
 340 GOTO 370
350 C[2*J-1,K+20]=P
 360 C[2*J,K+20]=V
 370 NEXT K
 380 NEXT J
 390 NEXT I
 400 FOR I=1 TO 41
 410 WRITE (15, 430) C[1, I], C[2, I]
 420 NEXT I
 430 FORMAT 4F10.5
 440 REDIM A[2,42]
 460 FOR K=1 TO 41
 470 A[1,K]=C[1,K]
```

Table 9 HP 9830A Program to Convert Data to Matrix Format for 1 Crystal (cont)

480 A[2,K]=C[2,K] 490 NEXT K 500 A[1,42]=A[2,42]=A[1,1] 510 STORE DATA #5,M,A 520 N=N+1 530 M=M+1 550 GOTO 70 560 DISP "S/N NOT ="; 570 END

# Table 10 HP 9830A Program to Calculate Coefficients for Crystal Detectors - Degree = 3

```
10 DIN CS[36], B[8], A[2,42]
20 REM PROGRAM TO CALCULATE CRYSTAL DETECTOR COEFFICIENTS
 30 DISP "FIRST FILE #, # OF FILES";
40 IMPUT N1,N2
 50 FOR L=0 TO N2-1
 60 MAT C=ZER
70 MAT B=ZER
80 B[1]=1
90 W=N=S1=S2=S3=S4=S5=0
100 D1=D2=3
110 LOAD DATA N1+L,A
120 FIXED 6
130 FOR H=2 TO 47
140 B[2]=LGT(A[2, H])
150 Y=LGT(A[1,H])
160 FOR I=2 TO D2
170 B[I+1]=B[I]*B[2]
180 NEXT I
190 B[ D2+2 ]=Y
200 R=0
210 FOR I=1 TO D2+2
220 FOR J=I TO D2+2
230 R=R+1
240 C[R]=C[R]+E[I]*B[J]
250 NEXT J
260 NEXT I
270 S1=S1+B[2]
280 S2=S2+B[2]^2
290 S3=S3+Y
300 S4=S4+Y^2
310 S5=S5+B[2]*Y
320 N=N+1
330 NEXT H
340 D1=3
350 IF W=0 THEN 830
360 T=0
370 FOR I=1 TO D1+1
330 B[I]=0
390 FOR J=1 TO D1-I+2
400 R=(I+J-1)*(D2+2-0.5*(I+J))
410 B[I]=B[I]+C[T+J]*C[R]
420 NEXT J
430 T=I*(D2+(3-I)/2)
440 NEXT I
450 R1=0
460 FOR I= 2 TO D1+1
470 R1=R1+C[I*(D2+(3-I)/2)]^2
```

## Table 10 HP 9830A Program to Calculate Coefficients for Crystal Detector - Degree = 3 (cont)

```
480 NEXT I
490 TO=C[(D2+1)*(D2+2)/2]
500 TO=TO-C[D2+1]^2
510 FOR I=1 TO 3
520 PRINT
530 NEXT I
540 PRINT " ", "S/N ="A[1.1]: "SECOND CALIBRATION"
550 PRINT
560 PRINT
570 PRINT " ". "COEFFICIENTS"
580 PRINT
590 FORMAT 12X, F2.0, F12.7
600 FOR I=1 TO D1+1
610 WRITE (15,590)"B("I-1")="B[I]
620 NEXT I
630 PRINT
640 PRINT
650 PRINT " ", "R SQUARE ="R1/TO
660 PRINT
670 PRINT " ", " VOLTS", "MILLI WATTS", " Y' "." ERROR(%)"
680 Q=0
690 FOR I=2 TO 41
700 X1=A[2,I]
710 Y1=A[1,I]
720 Y2=10^(B[1]+B[2]*LGT(X1)+B[3]*(LGT(X1))^2+B[4]*(LGT(X1))^3)
730 Q = Q + ((Y1 - Y2)/Y1)^2
740 PRINT " ", X1, Y1, Y2, 100*(Y1-Y2)/Y1
750 NEXT I
760 PRINT
770 PRINT
780 PRINT " ". "RMS ERROR ="100*SQR(Q/40)"PERCENT"
790 FOR J=1 TO 6
800 PRINT
810 NEXT J
820 GOTO 1210
830 P= V=1
840 D2=D2+1
850 FOR J=1 TO D2
860 C[P]=SQRC[P]
870 FOR I=1 TO D2-J+1
880 C[P+I]=C[P+I]/C[P]
390 NEXT I
900 R=P+I
910 S=R
920 FOR I=1 TO D2-J
930 P=P+1
940 FOR M=1 TO D2+2-J-I
```

Table 10 HP 9830A Program to Calculate Coefficients for Crystal Detectors - Degree = 3 (cont)

```
950 C[R+M-1]=C[R+M-1]-C[P]*C[P+M-1]
960 NEXT M
970 R=R+M-1
980 NEXT I
990 P=S
1000 NEXT J
1010 T=(D2+1)*(D2+2)/2
1020 FOR I=1 TO D2-1
1030 T=T-1-I
1040 C[T]=1/C[T]
1050 FOR J=1 TO D2-I
1060 P=D2+1-I-J
1070 P=P*(D2+1-(P-1)/2)-I
1080 R=P-J
1090 S=O
1100 U=I+J+1
1110 V=P
1120 FOR K=1 TO J
1130 V=V+U-K
1140 S=S-C[R+K]*C[V]
1150 NEXT K
1160 C[P]=S/C[R]
1170 NEXT J
1180 NEXT I
1190 C[1]=1/C[1]
1200 GOTO 360
1210 NEXT L
1220 END
```

Table 11 General Fixture Calibration Program (HP 9810A) - 16 Pins

19900 - CI k 20		
6491 K55	005171040	0101- 456
0002CLX37	0052D1V35	0102 L60
0003FMT42		0103 a13
	0053 N73	
0004FMT42	0054FMT42	0104FMT42
0005 E60	0055STP41	0105STP41
UU06 N73	0056XT023	0106 101
PH07XT022	0057 101 ,	0107XT023
0008 E60	0058 000	0108 a13
คืบ09 ฉโ3	0059 810	0109FMT42
0010CNT47	0060PNT45	0110 404
0011 D63	0061INT64	0111 101
0011 003		0112FMT42
0012 A62	0062 UP27	
0013XT023	0063EEX26	0113 101
0014 A62	0064 202	0114FMT42
0015CNT47	0065DIV35	0115PSE57
0016 C61	0066 DN25	0116PSE57
0017 A62	0067 UP27	0117PSE57
0018 a13	0068INT64	0118CNT47
0019 D63	006934	0119CMT47
0020FMT42	0070EEX26	0120LFL51
0021CNT47	0071 202	0121 C61
	0072 X36	0122FMT42
0922FMT42		0123 303
0023XFR67	0073YT040	0124 303
0024FMT42	0074 810	012521
0025FMT42	0075 911	
0026 F16	0076FMT42	6126 UP27
0027 a13	0077 404	0127FMT42
0028 E60	0078 101	0128 404
U029 b14	0079FMT42	0129 101
003021	0080SFL54	0130FMT42
0031CNT47	0081FMT42	0131 101
Пи32SFL54	0082CHT47	0132FNT42
H633FMT42	0083FMT42	0133 o13
0034XFR67	0084FMT42	0134 UP27
0035 000	0085YT040	0135XFR67
0036PNT45	0086 E60	0136 810
0037 101	0087XT03°	0137 911
	0088CNT47	0138X=Y50
0038XT023	0089 «56	0139 DN25
0039000		0140GTO44
0940CLX37	0090071	0141LBL51
0041XT023	0091IND31	
0042 101	0092 E60	0142 D63
0043 911	0093 a13	0143 101
0044XT023	0094CNT47	9144 7 97
0045 202	0095 A62	0145X=Y50
0046 000	0096 N73	0146 DN25
0047LBL51	0097 D63	0147GTO44
0048 B66	0098CLR20	0148LBL51
0049FMT42	0099 156	0149 D63
0050FMT42	0100 A62	0150 DN25

# Table 11 General Fixture Calibration Program (HP 9810A)- 16 Pins (cont)

(1) 5 1 = 1 = 1 = 1 = 1 = 1 = 1 = 1 = 1 = 1	in Cerus	
017226	0201	0250 110047
9103CH832	0202CHT47	0252 NT47
	0203 10)	0253 161
0154 303	0204XTO28	0254 8 10
9155X>Y53	0205 +33	
017601837	0206 ь14	<b>0255 UP</b> 27
H157XEY30	0207XFR67	0256 a13
0158CHT47		0257XKY52
11159CNT47	0208IND31	0258PSE57
	0209 ь14	025967044
0160LBL51	0210 UP27	0260LBL51
U161 D63	0211INT64	0261 C61
U162 IIH25	0212 34	
0+03 K55	0213 UP27	0262XFR67
0164 4 94	0214EEX26	0263 101
0165xto23		0264 707
0166 810	0215 707	0265XT023
	0216DIV35	0266D[V35
и <u>167</u> 810	0217RUP22	0267 101
U168 a13	0218XEY30	0268 000
11169 UP27	0219XFR67	
0176 2 02	0220 8 10	0269 606
11171 836		0270CNT47
0172 101	0221 8 10	0271 810
01/3 91i	0222 X36	0272 911
	0223 X38	0273XFR67
0174 +38	0224RUP22.	0274 +33
0175YT040	0225XEY30	0275 810
0176 614	0226 X36	
0:77XFR67	0227 X36	0276 911
0178IHD31	PAGE IT A TT-JB	0277XT023
0179 b 14	0228 X36	0278 6 14
U180 UP27	0229 DN25	0279MFR61
	0230 +33	0280 101
0:31INT64	0231 YE24	0281 810
018234	9232 +33	0282XT028
U132 UP27	0233 81A	
U134EEX26	0234 7 07	0283IND31
H135 5 <u>45</u>	0235 DN25	0284DIV35
0136DIV35		0285 b <b></b> 14
0187 DN25	0236 K55	0286 911
0138XEY30	0237 505	0287 000
	0238 UP27	0288XT023
0189 UP27	0239 810	0289 o13
0190 101	0240 911	0290CLX37
0191 000	0241XFR67	
9192 X36	0242 +33	0291 UP27
0193XFR67		0292LBL51
0194 8 10	0245 a13	0293 E60
0195 810	0244XT028	0294XFR67
	0245 614	0295[N])31
M196 X36	0246YTO40	0296 a13
0197 DN25	0247IND31	0297 +33
3198 +33	0248 b14	
U199	0249 101	0298 101
6260 ··· 910		0299 E <b></b> -60
	0250 E60	0300!01

# Table 11 General Fixture Calibration Program (HP 9810A)- 16 Pins (cont)

	U.U1 - 6 00	0351-001147	04
	0302 6 06	0352	0401 ;01
	0303 UP27	0353 404	0402- TU23
			0403 614
	0304 a13	0354810	0404LBL51
	0365X <y52< td=""><td>0355FMT42</td><td>0405 F16</td></y52<>	0355FMT42	0405 F16
	ს306 DN25	0356YT040	0406FMT42
	0307GTO44	0357DIV35	0407 404
	0308LBL51	0358 N73	0408 21
	6.09 E60	0359CMT47	0409 4 04
	0519 DN25	0360 UP27	041021
	0311YT040	036134	0411 000
	0312 101	0362 UP27	0412 614
	0313 000	0363PNT45	341342
	0314 707	0364CLR20	0414 4 64
	0315FMT42	0365SFL54	0415 8 10
	0316 404	0366XEY30	0416PNT45
	0317 810	0367CLR20	
	0318FMT42	0368 n56	0417CMT47
			0418 -FMT40
	0319CLR20	0369 071	0419 404
	0020SFL54	0370 o13	042021
	00021 UP27	0371XT023	0421 101
	0022 DN25	0372CNT47	0422 7 07
	0323CLR20	0373CNT47	0423 ,21
	8024 UP27	0374CNT47	0424 4 99
	0325CNT47	0375CNT47	8425XFR67
	0326CNT47	0376CNT47	0426IND31
	0327CNT47	0377CNT47	0427 a13
	0328CNT47	0378CNT47	0428FMT42
	0329CNT47	0379 M70	0429 4 20-03
	U330CNT47	0380 I65	0430 810
	0331CNT47	0381 L72	0431FMT42
	0232CNT47	0382 L72	0432PNT45
	0333CNT47	0383 165	0433CLR26
	0334CNT47	0334IND31	0434SFL54
	0335 UP27	0385 A62	0435XEY3A
	0336IFG43	0386XT023	0436FMT48
di	0337FMT42	0387XTO23	
		0388YTO40	0437 101
	0338CNT47		0438 UP27
	0339FMT42	0389CMT47	0439 E60
	0340 404	0390 071	04-9 161
	034121	03911/X17	0441 707
	0342 101	0392XTQ23	0442 UP27
	0343 000	0393CLR20	0443 614
	034421	0394SFL54	0444X <y52< td=""></y52<>
	0345 303	0395XEY30	0445GTO44
	0346CNT47	0396FMT42	0446LBL51
	0347XFR67	0397 911	0447 F 16
	0348 101	0398 006	0448CHT47
	0349 000	0399	0449 - XFR67
	0350 810	0400 a13	0450 - 1 01

# Table 11 General Fixture Calibration Program (HP 9810A) - 16 Pins (cont)

(cont)		
0451-000	0501 671	0551 67
0452 606	0502:HP31	0552 016
0453FM142	0503 E60	0553FMT42
0454 4 04	0504 a13	0554CNT47
045521	0505CNT47	0555 UP2
0456 101	0506 071	
0457 000		0556 M70
045821	05071/X17	0557 UP27
	0508XT023	0558IND %i
0459 404	0509CNT47	0559CLR20
0460FMT42	0510 UP27	0566SFL54
0461 404	051134	0561CLR
0462 810	0512 UP27	0562XEY
0463FMT42	0513FMT42	0568 L 7
0464CLR20	0514XFR67	0564071
0465 I65	0515 101	0565YTO 13
0466 N73	0516 000	0566YT0
0467 C61	0517 606	0567 UP27
0468 I65	0518 UP27	0568 816
0469 D63	0519XFR67	0569 D63
0470 E60	0520 101	0570 UP27
0471 N73	0521 000	0571 B60
0472XT023	0522 707	
0473CNT47	0523DIV35	0572 UP27
0474 n56		0573 911
0475 071	0524XEY30	0574 UP27
0476IND31	0525 K55	0575CHT47
	0526 4 04	0576 UP27
0477 E60	0527 UP27	057734
0478 a13	0528 505	0578 FMT 42
0479CHT47	0529 X36	0579XFR67
8480 UP27	0530YT04u	0580IND31
048134	0531IND31	0581 0 0A
0482 UP27	<b>05</b> 32 000	0582FHT42
0483CNT47	0533YT040	0583
U484PNT45	0534 +33	0584 810
0485CNT47	0535 101	0585PNT45
0486 UP27	0536 911	0586CNT47
0487 M79	0537 DN25	0587FMT42
0488 UP27	0538 UP27	0588 5 05
0489IND31	0539XSQ12	0589FFX26
0490CLR20	0540XT023	0590FMT43
0491SFL54	0541 +33	8591FMT42
0492XEY30	0542 202	0592 013
0493CLR20	0543 000	0593 E60
6494XT023	0544RUP22	0594 C61
0195 071	0545FMT42	0595 071
0496XT023	0546 4 04	0596 a13
0/97 969	0547 8 10	0597 D63
0498 L72	0548PNT45	
0499CNT47		05981FG43
0500 (56	0549CHT47 0550CHT42	059942
0300 " "36	0000-111142	0600 31841

# Table 11 General Fixture Calibration Program (HP 9810A)- 16 Pins (cont)

(cont)		
11601 - 1 61	065] [60	070! 4 04
0602 911	0652111731	070221
4603 UP27	0653CNT47	0703 404
0604 911	0654 156	070421
0605 000	0655 A62	0705 066
0606FMT42	Ø656 π56	9706 010
0607 505	0657 E60	0707FMT42
0608XT023	0658 α13	6766 3 H4
11609 101	0659FMT42	0709816
0610XTO23	0660STP41	0710PHT45
0611 +33	0661FMT42	0711CHTJ7
0612 000	0662 4 04	0712-FMT42
0613CNT47	0663 810	0713 4 04
1614 101		
0615 707	0664FMT42	07142; 0715 101
9616 UP27	0665CLR20	
	0666SFL54	0716 4 04
0617XFR67	0667XEY30	071721
0618 000	0668 n56	0718 4 4-04
0619X <y52< td=""><td>0669 071</td><td>2719-WFR67</td></y52<>	0669 071	2719-WFR67
0620GTO44	0670 a13	0720IND31
0621LBL51	0671KTO23	0721 a10
9622 B66	0672CNT47	0722FMT42
U623CMT47	0673CHT47	0723 405
0624XFR67	0674CNT47	0724 810
0625 101	0675CHT47	0725FMT42
0626 911	0676CNT47	0726PNT45
9627 UP27	0677CNT47	0727CLR20
8628 101	0678CNT47	0728SFL54
0629 606	0679 L72	0729XEY30
0630DIV35	0680 071	0730FMT42
9631YT040	0681YT040	0731 101
··· 32 101	0682YT040	0732 E60
- 0 33 9 <b>1</b>	0683 UP27	0733 101
10 34 YE24	0684 810	0734 707
10:35 202	0685 D63	0735 UP27
0636 000	0686 UP27	0736 a13
1163751V35	0687 B66	0737X <y<b>52</y<b>
0638XFR67	0688 UP27	0738GTO44
0639 101		0739LBL51
Un40 911	0690 UP27	0740 G15
0641XSQ12	0691CLR20	0741CNT47
064234	0692SFL54	0742FMT42
n: 43 DN25	0693XEY30	0743 404
ne44 r76	0694FMT42	074421
0645XTO23	0695 101	0745 911
(0.46 202	0696XT023	074621
9647 000	0697 a13	0747 404
0648FMT42	G698LBL51	0748CNT47
0649FMT42	0699 G15	0749 - FRT42
0659 II73	0790FMT42	0756 4 04

## Table 11 General Fixture Calibration Program (HP9810A)- 16 Pins (cont)

0751	1.0
9752	4 O
U753CLR	2.0
	70
0755 E	
	50
0756 A	
	73
U258CHT	
	27
	34
0761FMT	42
0762CNT	47
0763XFR	
	31
	1 1
M766FMT	12
W767 4	34
0768 8	10
0769FMT	
0770PMT	15
0271CLR;	20
0772SFL	5.4
11773XEY	9 G
0774CLR	2 W 2 M
0775YTQ	10
	1.63
0/79 p(	
0780 Ae	
0781 - g	
0/82 D	
0783CMT	
9784 E(	
	13
0786 ()	13
0787 0	7 1
0788 a:	13
0789CNT	17
0290 HP	20 727
0791	9 4
0791 0792	12
1794XFP	7
0794XFR6 0795 26	10
й796 Öİ	i ii
0797РМТ2	10
0740 4 0	र केल वे औ
0798 40	J 14 L (3)
0799 81	10
	4 .**

0801 FAT45
0802CLR20
0803SFL54
0804XEY30
0805CLR20
6306 A69
0306 A62 0807 B66
0808VTO40
0808YT040 0809 071 0810 L72
0007 0 1
08111/X17
00111/A1/
0812XT023
0813 E60
0814CNT47
0815 L72 0816 071
0816 U/1
0817YTO40
0818YTO40
0819CMT47
0820 F16 0821 A62
0821 A62
- 0822 U61
- M823XTO23
0824 071
0824 071 0825 a13
6856CN147
0827 UP27
082834
0829FMT42
0830XFR67
0831 101
0831 101 0832 911 0833 UP27 0834 101
0833 UP27
0834 101
0835 000
0836DIV35
0837 DN25
Ø₹38 K55
0839 505
0840FHT42
0841 4 04
0841 404 0842 810
0843PNT45
0844CNT47
0845FMT42
0846FMT42
0847 N73
0040 060
0848 E60 0849 YE24
0850XTG23
0000 UIO

0851 0	11 47
0852	F16
0853	013
0854	E 60
0855	b14
0856	H
0857F	
0858	
0859E	HD46

Table 12 General Fixture Calibration Program Data Register Allocation

a	CHANNEL	COUNTER

9

### Table 12 (Continued)

		( continued)						
24	DETECTOR	COEFFICIENTS	B <sub>2</sub>	&	B <sub>3</sub> -	DETECTOR	#	2
25			B <sub>0</sub>	&	B <sub>1</sub>			3
26			B <sub>2</sub>	&	B <sub>3</sub>			3
27			Bo	&	В			4
28			B <sub>2</sub>	&	B <sub>3</sub>			4
29			Bo		107710			5
30			B <sub>2</sub>	&	B <sub>3</sub>			5
31			Bo	&	B <sub>1</sub>			6
32			B <sub>2</sub>	&	B <sub>3</sub>			6
33			Bo					7
34			B <sub>2</sub>					7
35			Bo		The second			8
36			B <sub>2</sub>	&	B <sub>3</sub>			8
37			B <sub>O</sub>	&	B <sub>1</sub>			9
38			B <sub>2</sub>	&	B <sub>3</sub>			9
39			Bo	&	B <sub>1</sub>			10
40			B <sub>2</sub>	&	B <sub>3</sub>			10
41			Bo	&	В			11
42			B <sub>2</sub>					11
43			Bo	&	B <sub>1</sub>		6	12
44			B <sub>2</sub>	&	B <sub>3</sub>			12
45			B <sub>O</sub>	&	В			13
46			B <sub>2</sub>	&	B <sub>3</sub>			13
47			B <sub>0</sub>	&	В		y L	14
48			B <sub>2</sub>	&	B <sub>3</sub>			14 .
49			B <sub>0</sub>	&	B <sub>1</sub>			15

### Table 12 (Continued)

73

74

75

SPARE

SPARE

SPARE

50	DETECTOR	COEFFICI	ENTS -	B <sub>2</sub>	&	B <sub>3</sub>	DETECTO	OR #	15
51				B <sub>0</sub>	&	B <sub>1</sub>			16
52				B <sub>2</sub>	&	B <sub>3</sub>			16
53				Bo	&	В			17
54				B <sub>2</sub>	&	B <sub>3</sub>			17
55	SPARE								
56	SPARE								
57	SPARE								
58	SPARE								
59	SPARE								
60	SPARE								
61	SPARE								
62	SPARE								
63	SPARE								
64	SPARE								
65	SPARE								
66	SPARE								
67	SPARE								
68	SPARE								
69	SPARE								
70	SPARE								
71	SPARE			30					
72	SPARE								

### Table 12 (Continued)

- 76 SPAKE
- 77 SPARE
- 78 SPARE
- 79 SPARE
- 80 SPARE
- 81 SPARE
- 82 SPARE
- 83 SPARE
- 84 SPARE
- 85 SPARE
- 86 SPARE
- 87 TEMPORARY STORAGE FOR CALCULATING P
- 88 LOG V
- 89 INPUT PORT
- 90 POWER OUT OF PORT # 1
- 91
- 92
- 93
- 94 5
- 95 6
- 96
- 97
- 98 9
- 99 10
- 100
- 101 12

#### INTEGRATED CIRCUIT SUSCEPTIBILITY

MDC E1099 12 JULY 1974

		4
Table	77	[Continued]
IGNIC	16.	(Continued)

	(00	
102	POWER OUT OF PORT	13
103		14
104		15
105		16
106	INCIDENT POWER	
107	TOTAL POWER OUT	
108	S/N	

Table 13	Dissipat 16 Pin D 0.22 GHz	ion Loss Data for IP Test Fixture at	Table 14	Dissipation Loss Data for 16 Pin DIP Test Fixtur at 0.91 GHz	3
	100 110 110 110 110 110 110 110 110 110	10SS(d3) 0.1750 0.1715 0.1522 0.1693 0.1833 0.1734 0.1734	Manual 100m では、10m4naとのの011に下れて	LOSS(43) 0.5317 0.4721 0.4727 0.5139 0.4787 0.5713 0.4221 0.4409 0.5746 0.5008	
	11	- 9	11	0.4791	
	DARD	3RROL = 0.0262	STAIDARD ER	ERROR = 0.0839	
	ABSOLUTE 3	ABSOLUTE LOGS FACTOR = 1.0374	ABSOLUTE LO	IO33 FACTOR = 1.1166	

16 Dissipation Loss Data for 16 Pin DIP Test Fixture at 5.6 GHz	10058(43) 1	MEAN = 0.9044	STANDARD ERROR = 0.25:2	ABSOLUTE LOSS FACTOR = 1.2515
Dissipation Loss Data for 16 Pin DIP Test Fixture at 3 GHz	1033(23) 0.1611 0.2371 0.2189 0.1635 0.1989 0.2547 0.2077 0.2077 0.2376 0.2496 0.2496	0.1970	STANDARD ERROR = 0.0319 ST	ABSOLUTE LOSS FACTOR = 1.0464 AE
Table 15	MO H - 2 と 4 で 6 と 8 を 6 上 5 む 4 で 6 と 8 を 6 上 5 む 4 で 6 と 8 を 6 上 5 む 4 で 6 と 8 を 6 と 5 む 4 で 6 と 8 を 6 と 8	NEAN =	STAN	ABSO

Q	
Sipa	-
SO	3
S	,
10	
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ap	
10	

7 4	3
for	U
n Loss Data for	
Los	ב ב
Dissipation	
E.	5
0 5	= = =
SS	
015	9.1
188	7

ss Data for t Fixture at	
Dissipation Loss Data for 8 Pin TO-5 Test Fixture at 0.22 GHz	LOSS(4B) 0.1519 0.8181
Table 18	PORT 2

1053(dB) 0.5559 0.5559 0.7084 0.5672 0.6015 0.6015 0.4697 0.5247 0.6945	0.7089
EEC 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	NEW =

ABSOLUTE LOSS FACTOR =

0.2661

STANDARD ENROR =

Table 19	Dissipation Loss Data for 8 Pin TO-5 Test Fixture at 0.91 GHz	Table 2	O Dissipation Loss Data for 8 Pin TO-5 Test Fixture at 3 GHz
PORT LOSS(  1 0.41 2 1.01 3 0.56 4 0.40 5 0.37 6 0.41 7 0.43 8 0.43	50 25 63 30 97 32	PORT 1 2 3 4 5 6 7 8	LOSS(dB) 0.3019 0.6478 0.3319 0.2966 0.2757 0.3976 0.4162 0.3973
MEAN = 0.5068		MEAN =	0.3831
STANDARD ERROR =	0.1983	STANDARD	ERROR = 0.1117
ABSOLUTE LOSS FA	CTOR = 1.1238	ABSOLUTE	LOSS FACTOR = 1.0922
Table 21	Dissipation Loss Data for 8 Pin TO-5 Test Fixture at 5.6 GHz	Table 22	Dissipation Loss Data for 8 Pin TO-5 Test Fixture at 9.1 GHz
PORT LOSS (6 1 0.694 2 1.155 3 0.830 4 0.946 5 0.830 6 1.135 7 0.922 8 0.932 MEAN = 0.9311	1 59 08 58 08 69	PORT 1 2 3 4 5 6 7 8	LOSS(dB) 2.3016 1.7793 1.8986 2.0717 2.1899 2.6554 2.4368 2.6065
STANDARD ERPOR =	0.1454	MEAN =	2.2425
ABSOLUTE LOSS FAC			ERROR = 0.2977
ADOUGLI DOOS FAC	TOR = 1.2391	ABSOLUTE	LOSS FACTOR = 1.6759

### TABLE 23 EXAMPLE OF 741 INTERFERENCE SUSCEPTIBILITY DATA

S/N = 330

P(mW) -0.0001 0.0384 0.0596 0.0851 0.2514 0.4498 0.9689 1.6265 3.0516 10.5494 18.5502 34.0799 54.5367 103.4030 134.7200 198.5100 277.1050 396.2030 521.0260 760.4520	C.F.(dB) 0.000 2.253 2.229 2.493 2.519 2.530 2.508 2.512 2.496 2.446 2.419 2.383 2.354 2.453 2.355 2.209 2.085 1.961 1.867 1.713	VOUT -4.927 -4.988 -5.019 -5.068 -5.380 -5.772 -6.652 -7.564 -8.912 -8.993 -8.972 -8.922 -8.843 9.829 9.732 9.506 9.195 8.721 8.186 7.254	10UT 9.85 9.98 10.04 10.14 10.76 11.54 13.30 15.13 17.82 17.94 17.84 17.69 -19.66 -19.46 -19.01 -18.39 -17.44 -16.37 -14.51	0.00 0.00 -0.00 -0.00 -0.00 -0.00 -0.00 0.00 0.00 0.00 0.00	INI -0.0106 -0.0110 -0.0112 -0.0111 -0.0112 -0.0112 -0.0111 -0.0109 -0.0108 -0.0108 -0.0081 -0.0099 -0.0107 -0.0109 -0.0109	-11.82 -( -11.82 -( -11.81 -( -11.80 -( -11.78 -( -11.75 -(	0.04 42 0.04 38 0.0054 0.0054 0.0056 0.0060 0.0064	VON6 -11.82 -11.82 -11.82 -11.81 -11.81 -11.80 -11.78 -11.72 -11.72 -11.72 -11.72 -11.72 -11.94 -11.94 -11.94 -11.94
P(mW) -0.0001 0.0384 0.0596 0.0851 0.2514 0.4498 0.9689 1.6265 3.0516 10.5494 18.5502 34.0799 54.5367 103.4030 134.7200 198.5100 277.1050 396.2030 521.0260 760.4520	ION 6 -0.0278 -0.0280 -0.0284 -0.0286 -0.0298 -0.0316 -0.0356 -0.0356 -0.0446 -0.0454 -0.0452 -0.0454 -0.0052 -0.0054 -0.0058 -0.0066	VCC+ 11.93 11.93 11.93 11.93 11.93 11.93 11.93 11.93 11.93 11.93 11.71 11.71 11.71 11.71 11.75	ICC+ 0.80 0.80 0.90 0.90 0.90 1.30 0.90 1.00 0.90 1.00 0.90 21.70 21.40 20.70 19.80 18.20	VCC11.84 -11.84 -11.84 -11.83 -11.82 -11.80 -11.77 -11.74 -11.74 -11.74 -11.96 -11.96 -11.96 -11.96	ICC11.50 -11.80 -11.70 -11.80 -12.50 -13.40 -15.40 -17.70 -20.30 -20.50 -20.50 -20.50 -20.60 -0.70 -0.90 -1.00 -1.10	1.4130 1.5130 1.7090 1.9090 2.1450	III 0.4940 0.4996 0.5024 0.5068 0.5353 0.5708 0.6510 0.7338 0.8618 0.8688 0.8618 0.8688 0.8618 0.8618 1.0157 -1.0157 -1.2117 -1.4117 -1.6477 -1.8287 -2.0636	

ALL VOLTAGES IN VOLTS
ALL CURRENTS IN MILLIAMPS

IUDIC	LT /TOO LINCE ICICINCE ICSC I	logium (mooron)
-0000CLR20		
0001FMT42	0051 202	0101XFR
0002XFR67	0052 404	0102 1

. BODD OF BLANK		CONTROL OF THE OWNER,
0001FMT42	0051 202	0101XFR67
0002XFR67	0052 404	0102 101
0003XFR67	0053CLX37	0103 606
0004 202	0054XT023	
0005 404		0104 UP27
	0055 303	0105INT64
0006PNT45	0056 202	010634
0007LBL51	0057XT023	0107 UP27
0008 A62	0058 404	0108EEX26
0009FMT42	0059 101	0109 505
0010 404	0060LBL51	0110DIV35
0011 101	0061 B66	0111RUP22
0012FMT42	0062FMT42	0112XEY30
0013SFL54	0063 4 04	
0014FMT42	9964 191	0113 101
0015PSE57		0114 000
	0065FMT42	0115 X36
0016FMT42	0066 101	0116 DN25
0017FMT42	0067FMT42	0117XT023
0018YTO40	0068STP41	0118 404
0019DIV35	0069 101	0119 606
0020 N73	0070XTO23	0120YT040
0021FMT42	0071 a13	0121 4 04
0022STP41	0072SFL54	0122 5 05
0023XTO23 .	0073LBL51	0123XFR67
0024 303	0074 C61	
0025 000	0075FMT42	0124 101
0026PNT45		0125 707
	0076 303	0126 UP27
0027 UP27	0077 303	0127INT64
0028EEX26	007821	012834
0029 303	0079 UP27	0129 UP27
0030DIV35	0080FMT42	0130EEX26
0031 DN25	0081 404	0131 707
0032 UP27	2082 101	0132DIV35
0033INT64	0083FMT42	0133 DN25
003434	0084 101	0134CHS32
v035 101	0085FMT42	
0036 000	0086 101	0135XT023
	0087 505	0136 404
0037 X36		0137 810
0038 DN25	0088 UP27	0138YT040
0039INT64	0089 a13	0139 404
0040 UP27	0090X>Y53	0140 707
0041 101	0091GTO44	0141XFR67
0042XTO23	0092LBL51	0142IND31
U043 202	0093 I65	0143 a13
0044 3 03	0094CNT47	0144 UP27
0045X=Y <b>5</b> 0	0095RUP22	0145 4 04
0046CNT47	0096 K55	
0047 101	0097 404	0146 5 05
	0098XT023	0147XT023
0048 000		0148 614
0049 +33	0099 202	0149LBL51
0050YTO40	0100 606	0150 D63

	Table	24	7400 Interference	Test Pro	ogram (HF	9810A)
0151-6 044			(cont) 0201 - 610		0251	114
0152 1-77			020234	S-300	0252	DN29
0153LBL51			0203 DN25			7T040
0154 H74			0204 K55			IND31
0155XT028			0205 505			6 14
0156JHD31			0206 UP27			
015734 0158 b14			0207 101			LBL51 J75
0159 1 01			0208 505			LBL54
0160XTO23			0209 UP27 0210 013			
016133			0210 0 13 0211X(Y52			2 01
0162 b14			0212GTO44		0262	303
#163 4 04			0213LBL51			XEY30
0164 911			0214 E60			9 11
0165 UP27			0215CNT47			XFR67
0166 5 14			0216XFF67			X36 202
0167X <y52 0168 DN25</y52 			0217 0 00		0207	3 63
0169GTD44			0218INT64 0219XEY30		0269	+33
· 9170LBL51			0217-76126			YT040
0171 0 63			0221 6 06			2 02
0172XFR67			0222DIV35			5
0173 202			0223 DN25			DH25
0174 6 06			0224DIV35		-	XFR67
0175XTO23			0225 101			101
0176 6 14			0226 8 10			816 X36
0177XFR67 0178 X36			0227XFR67			5 05
0179 4 <b></b> 04			0228 +33 0229 202			UP27
0180 6 06			0230 4 04			013
0181XFR67			0231XTO23			X <y52< td=""></y52<>
0182 + 30	•	**	0232 b14			GT04%
0183 4 04			0233 YE24			LBL51
0184 5 05			0234IND31		- 1	G15
0185 UP27			0235DIV35			CHT47
0186 b14			0236 514			XEY30 101
- 0187XSQ12 - 0188XFR67			0237 YE24			1 91
0189 X36			0238DIV35 0239 101			x≐Y50
0190 402			0240 810	A.		GT044
0191 7 07			0241XFR67	7		LBL51
- 6192 430			0242 2 02			· G15
0193 61			0243 303			CHT47
0194XSQ12			0244 UP27			DH25
0195XFR6			0245 911			YT040
0196 %36			0246 X36			·IND31 · +33
0197 b10 0198XFR6			0247 202			
0199 X36			0248 202 0249 +33			- 4 35
0200 40			0250YT040			61044
	200		0200		FERRE	

## Table 24 7400 Interference Test Program (HP 9810A) (cont)

	rios inscribinde lese riogri	am (m solon) (conc)
0361LBL51	0351 J75	0401
0302 J75	0352 101	0402SFL54
0303LBL51	0353 E60 ·	0403FMT43
9304 G15		
	0354GTO44	0404 2 02
0305 101	0355LBL51	0405 303
0306 810	0356 C61	0406 UP27
0307XFR67	0357LBL51	0407 911
0308 +33	0358 I65	0408XFR67
0309 o13	0359 2 02	0409 X36
0310XT023	0360 202	0410 2 02
0311 b14	0361XEY30	0411 3 03
0312 DH25	0362 a13	0412 4 3)
0313 YE24	0363x>Y53	041341
0314IND31	9364GTO44	0414 a13
0315 X36	0365LBL51	
0316 614		0415XFR67
	0366 <u>a</u> 13	0416IND31
○317XFR67	0367CNT47	0417 a13
0318 202	0368P3E-+-57	0418CHS32
0319 404	0369PSE57	0419 UP27
0320 UP27	0370IFG43	0420 101
0321 α13	0371 DN25	0421CHS33
0322X=Y50	0372GTO44	0422 L
0323 DN25	0373LBL51	0423XFR67
0324GTO44	0374 L72	0424IHD31
0325LBL51	0375SFL54	0425 013
0326 F16	0376 DN25	0426 +33
0327 DN25	0377 YE24	0427YT040
0328YT040		
	0378IND31	0428IHD31
0329IND31	037934	0429 019
0330 <u>+</u> 33	0380 202	0430XEY30
0331 202	0381 505	0431DTV35
0332 505	0382L8L51	0432FMT49
0333GTO44	0383 L72	0433FMT42
0334LBL51	0384 101	0434·· π56
0335 J75	0385XTO23	0435CLR20
0336LBL51	0386 +39	0436IN764
0337 F16	0387 202	0437FMT42
0338XFR67	0388 5 05	0438PHT45
0339 000	0389YTO40	0439 DH25
์ ยั3 <b>40-</b> − มัค27	0390IND31	0440 K 55
0341INT64	0391 202	0441 4 61
<u> </u>	0392505	0442 UP27
0343 DM25	9393G1044	0443 1
0344DIV35	0394LBL51	0444 OO(
0345YTO40	0395 J75	0445 X36
0346IND31	0396LBL51	0446 1 01
0347 +33	0397 013	0447 E60
0348 2 02	0398FMT42	0448YT040
0249 505	0399 404	0449IHD31
0350LBL51	0400 101	0456 013
The first test that the first test to the first test test test test test test test t	0.100	

### Table 24 7400 Interference Test Program (HP 9810A)(cont)

U451- 5 ---05 0452-- E ---60 0453--XFR---67 0454--IND---31 0455-- a ---13 0456--PNT---45 0457-- 1 ---01 0458--XT0---23 0459-- + ---33 0460-- 2 ---02 0461-- 3 --- 03 0462--XFR---67 0463-- 2 --- 02 0464-- 3 --- 03 0465-- UP---27 0466-- 3 ---03 0467--%>Y---53 0468--GTO---44 0469--LBL---51 0470-- B ---66 0471--CNT---47 0472-- 1 --- 01 0473-- 9 ---11 0474-- UP---27 0475-- 3 ---03 0476-- 0 ---00 0477--FMT---42 0478-- 5 ---05 0479--XT0---23 0480--GT0---44 0481--LBL---51 0482-- A ---62 0483--LBL---51 0484-- H ---74 0485--EEX---26 0486-- 3 ---03 0487-- X ---36 0488-- DN---25 0489-- UP---27 0490--INT---64 0491-- - ---34 0492-- UP---27 0493--EEX---26 0494-- 4 --- 04 0495--BIV---35 8496-- DN---25 0497--8/8---77 0498--END---46

TIM", E4.0

7400 Data Tape to Matrix Tape Conversion Program for HP 9830A

Table 25

```
H
                                                                                                                                                                                                                     DOI
                                                                                                                                                                                                                    Vod
TG.B.
                                                                                                                                                                                                                     C.F. (43)
                            # OF FILES";
CON FS[20,9],A
DISP "FIRST NATRIX TAPE FILE";
                                                                                                                                                                                                                     P(mm)
                                                                                                                        # 1.6 = 1 10 20

# 1.6 = 10*# [1.4]

# 1.6 = 10*# [1.6]

# 1.9 = 100 0 [1.9]
                            **
             INFUT 0

DIESP "FIRST FILE #

INFUT W.H

FOR I=0 TO K-1

LOAD DATA HH, C

IF I>0 THEN 110

0 A=C[1]

10 IF A#C[1] THEN 45

10 FOR I=1 TO 9

                                                                                                                                                                                                                           MALIL (15, 310)"
FOR I=1 TO 20
                                                                                                                                                                                               FORTING
PRETER
                                                                                                                                                                                                                     PORTRE
                                                                                                                                                                          PRITE
PRITE
UCISH
```

Table 25 7400 Data Tape to Matrix Tape Conversion Program (cont)

WRITE (15, 350) F[I,1], F[I,2], F[I,3], F[I,4], F[I,5], F[I,6], F[I,7], F[I,8], F[I,9] FORIMT 5X, F10, 4, 2F8, 4, T8, 3, 4F8, 4, F8, 3 "S/N NOT ="A;C[1] DATA #5, Q GOTO 70 HENT I PRINT PRINT PRINT PRINT PRINT PRINT PRINT PRINT STORE G-0+1 END DI SP 

### Table 26 General Plot Program from Matrix Tapes for 7400 for HP 9830A

```
10 COM FS[20,9],A
 20 DIM C[19]
 30 DISP "FIRST FILE #":
 40 INPUT P
 60 LOAD DATA P
 70 SCALE 0,8.5,0,10
 80 OFFSET 2,1.5
90 XAXIS 0,1.5,0,6
 100 YAXIS 0,0.7,0,7
110 FOR J=0 TO 3
120 PLOT (LGT(2)+J)*1.5,0,1
130 LABEL (*,1,3.4,PI/2,7/6)
140 CPLOT 0,-0.3
150 LABEL (*)"-";
 160 PLOT (IGT(5)+J)*1.5,0,1
 170 CPLOT 0,-0.3
180 LABEL (*)"-";
 190 NEXT J
 200 DISP "YMIN, YMAX";
210 INPUT N.M
220 SCALE -7/3,10/3,N-1.5*(M-N)/7,N+8.5*(M-N)/7
230 FOR I=-1 TO 3
240 LABEL (*,1.5,1.7.0.7/6)
250 PLOT I, N, 1
260 CPIOT -2,-2
270 LABEL (310, 1.5, 1.7, 0, 7/6) 10;
280 CPLOT 0,0.6
290 LABEL (320,1.125,1.7,0,7/6)I;
300 NEXT I
310 FORMAT F3.0
320 FORMAT F2.0
330 IABEL (*,1.5,1.7,0,7/6)
340 A=(M-N)/5
350 FOR I=0 TO 5
360 PLOT -1, N+A*I, 1
370 CPLOT -7,-0.3
380 LABEL (400)N+A*I;
390 NEXT I
400 FORMAT F7.3
410 LABEL (*,1,0.8,0,7/6)
420 FOR I=1 TO 20
430 PLOT LGT(F[I,1]),ABS(F[I,7]),1
440 CPIOT -0.3,-0.3
450 LABEL (*)"*"
460 IPLOT 0, 0, 1
470 NEXT I
```

```
Table 26
                        General Plot Program from Matrix Tapes for 7400 for HP 9830A
480 PEN
                               (cont)
490 SCALE 0,8.5,0,10
500 OFFSET 2,1.5
510 FOR I=1 TO 4
520 PLOT I*1.5,0,1
530 PLOT I*1.5,7,2
540 NEXT I
550 FOR I=1 TO 10
560 PLOT 0, I*0.7, 1
570 PLOT 6, I*0.7, 2
580 NEXT I
590 PEN
600 SCALE =7/3,10/3,N-1.5*(N-N)/7,N+8.5*(N-N)/7
610 FOR Q=P+1 TO P+9
620 LOAD DATA Q
630 FOR I=1 TO 20
640 PLOT LGT(F[I,1]), ABS(F[I,7]), 1
650 CPLOT -0.3, -0.3
660 LABEL (*) "*"
670 NEXT I
680 NEXT Q
690 PLOT 0.15,7.5,1
700 LABEL (*)A
710 END
```

Table 27 HP 9810A 741 Interference Program

end@6 - [[[] 42	0019 )025	0098 203
4001 HFR67		0099 000
0002XFR67	005u	
9893 000	0051 101	0100XT023
	0052 707	0101 в14
14994PNT45	0053LBL51	0102XFR67
10095LBL51	0054 A62	0103IND31
1006 n56	0055FMT42	0104 b1
0007 101	0056 4 04	0105FMT42
0008XT023	0057 1 Ñ1	0106 404
0009 202	0058FMT42	0107 2 0;
na10 000		0108XT025
0011XFR67	0059SFL54	0109PSE57
UV12 505	0060FMT42	
0013 101	0061PSE57	0110PSE57
	0062PSE57	0111PSE57
0014FMT42	0063CLX37	0112 101
0015 404	0064XT023	0113XT020
0016 202	0065 707	0114 a10
0017XT023	0066 810	0115SFL54
0018FMT42	0067XT023	0116LBL51
\0019FMT42	0068 911	0117 B60
0020YT040	0069 404	0118FMT42
0021DIV35	0070CHT47	0119 3 03
10022 N73	0071 101	0120 3 0(
0023FMI42		012121
0024STP41	0072XT023	
0025XT023	0073 000	0122 UP27
- 3025 707	0074LBL51	0123FMT42
	0075 C61	0124 409
0027 606	0076FMT42	0125 101
0028PNT45	0077 404	0126FMT42
1029 UP27	0078 101	0127 101
0030EEX26	0079FMT4?	0128FMT42
0031 202	0080 101	0129 a10
0032DIV35	0081FMT42	0130 UP2
0033 DN25	0882XFR67	0131XFR6
6034 UP27	0083 7 07	0132 101
0035INT64	0034 3 03	0133 7 07
003634		0134X=Y50
0037 101	%095 UP27	0135 DN2!
0038 000	9036XFR67	0136GTO4
0039 X36	0087 202	
0040 DN25	0088 000	0137LBL51
	0089X=Y50	0138 M 70
+041INT64	0090GTO44	0139 1 01
0042 UP27	0091S/R77	0140 50
й043 505	0092LBL51	0141XEY30
H044XEY30	0093 013	0142X>Y53
0045X>Y53	0094 5 05	0143GT044
0046 UP27	9995 - A 00	0144LBL51
0047 4 04	0096 (TR- 67	9145 65
m048 +33	1007 1	0146011 47

## · Table 27 HP 9810A 741 Interference Program (cont)

and a state of the		0.00 A II TO 0.50
014 25	0196 - 1040	0245 1125
01115	0197 - 207	024625867
0149EEX26	0198 101	0247 101
0150CHS32	0199PSE57	0248 505
0151 3 03	0200 101	8249DIV35
0152X)Y53	0201XT023	11250 YE24
111:3CLX37	0202 +33	H251IND31
0154XEY30	0203 614	0252DIV35
-0355CHI47	0204XFR67	0259 1 01
9:56CHT47	0205IND31	<u> </u>
0.57LBL51	0206 ь14	0255XFR67
H:58 M70	0207 UP27	0256 000
n:199 pN25	0208INT64	U257 UP27
0160 K55	020934	0258 101
0151 4 04	0210 UP27	0259 6 06
0162XTO23	0211EEX26	0260 X36
8:63 1 01		11261 606
	0212 7 07	
0164 810	0213DIV35	0262 101
0:65 013	0214RUP22	u263 +33
9166 UP27	0215XEY30	0264YT040
u:67 2 <b>0</b> 2	0216XFR67	0265 614
u:68 X36	0217 101	0266 DN25
0:69 101	0218 810	026740
0170 911	0219 X36	0268IND31
11171 +33	0220 X36	0269 b14
0172YT040	0221RUP22	0270GTO44
· · · · · · · · · · · · · · · · · · ·		9271LBL51
0173 614	0222XEY30	
0174XFR67	0223 X36	0272 H74
0175IND31	0224 X36	0273L8L51
0176 614	0225 X36	0274 F16
0177 UP27	0226 DN25	9275 606
0178INT64	0227 +83	0276 202
U17934	0228 YE24	0277XEY30
0180 UP27	0229 +33	a278 101
0181EEX26	0230 707	ā279 6 <b></b> -06
0182 5 05	0231 101	9280XFR67
		0281 X36
0:83DIV35	0232 DN25	
U184 DW25	0233 K <b>5</b> 5	0282 000
0185XEY30	0234 505	928333-
0186 UP27	0235 UP27	9284YT040
0187 101	0236 101	0285 101
88 0 <b></b> 00	0237 505	0286 9 <b>-</b> 11
2189 X36	0238 UP27	9287 DN25
0190XFR67	0239 a13	0288 YÉ24
0191 101	0240XKY52	02891ND31
0192 810	0241GTO44	9290 X36
		0291 013
U193 X 36	0242LBL51	
8194 DH25	0243 F16	0292 XFR67
9195 +33	0244(11747	0290 301

### Table 27 HP 9810A 741 Interference Program (cont)

14:94 - 7 97	0843 1 75	039: -ini31
11295 1jp27	0344- / SFL54	
0296 a13	0345 DN25	0000 0 13
0297x=Y50	0346 YE24	0394CHS32
0298RUP22	0347IND31	0395 UP27
		9396 101
0399GTO44	034834	0397 D63
0030LBL51	0349 101	0398XFR67
0301 G15	0350 911	0399IND31
0302RUP22	0351LBL51	0400 - 013
0303GTO44	0352 J75	040133
U304LBL51	0353 101	0402 40
0305 N73	0354XT023	0403 1111 31
9396LBL51	0355 +33	
0307 G15	0356 101	0404 o13
из98XFR67	0357 911	0405XEY30
		0406DIV35
0309DIV35	0358YT040	0407FMT42
0310 101	0359IND31	0408FMT42
0311 606	0360 101	0409 1 56
MS12LBL51	0361 911	0410CLR20
0313 N73 .	0362GTO44	041164
0014XT023	0363LBL51	0412FMT42
0315IND31	0364 H74	041345
0316 +33	0365LBL51	
u317 101	0366 K55	0414 DH25
	0367XFR67	0415 K55
0318 911	0368 505	0416 404
0319LBL51		0417 UP27
0320 H74	0369 101	0418 101
0321 101	0370FMT42	0419 000
,0022 E60	0371 404	0420 X36
0323GTO44	0372 202	0421 1 01
0324LBL51	0373XT023	0422 E 60
0325 D63	0374FMT48	042071040
0336LBL51	0375 4 04	0424IND3:
0327 I65	0376 101	
0328 202	0377FM142	0425 a10
0329 911	Й378SFL54	0426 101
	0379FMT42	0427 E60
0030XEY30		0428XFR67
- 0331 α13	0380 101	0429IND31
0032X>Y53	0381 6 06	0430 a13
0333GTO44	0382 UP27	0431PHT45
u6.34LBL51	0383XFR67	0432 101
naas K55	10384 000	0433XT020
9336CNT47	0385 X36	0434 +30
0337PSE57	0386 605	
0338PSE57	0387 202	0435 0 00
9339IFG43	0388 +33	0436XT023
	0389YTO40	0437 +33
0340 DN25		0438 202
0341GT044	0390 a13	0439 - 106
0342LBL51	0391XFR67	0440 67

## Table 27 HP 9810A 741 Interference Program (cont)

0441- 008       0471- 04         0442- 0P27       0472- 0 -08         0443- 303       0473-X=Y56         0443- 303       0473-X=Y56         0445- GT044       0475-LBL51         0445- LBL51       0476- m -58         0447- CNT47       0478-GT044         0448- CNT47       0478-GT047         0448- GT047       0479-LBL51         0459- FMT42       0480- H -68         0451- EEX26       0481-LBL-51         0452- FMT42       0482- 0 -13         0453- FMT42       0483- XFR-63         0455- E -60       0485- 1 -63         0457- FMT42       0486- FMT-43         0458- STP41       0488- 2 -63         0459- 3 -03       0490- FMT-43         0460- 3 -03       0490- FMT-44         0463- 6 -06       0493- M -7         0463- 6 -06       0493- M -7         0465- 5 -05       0496- STP-44         0465- 5 -05       0497- S/R-7         0466- XTO-23       0497- S/R-7         0468- 1 -00       0498- END4         0499- STP4       0498- END4         0498- END4       0498- END4		
9442	11441- 11 99	047102
04433      03       0473X=T06         0444X>Y53       0474GT044         0445GT044       0475LBL51         0446LBL51       0476 n56         0447CNT47       0478GT046         0449FMT42       0479LBL51         0450505       0480R63         0451EEX26       0481LBL51         0453FMT42       04820-13         0453FMT42       0483XFR63         0453FMT42       0483XFR63         0455E60       04351-01         0457FMT42       0486FMT43         0459303       0496FMT43         0459303       0490FMT43         0460303       0490FMT43         04610927       0491FMT43         0463606       0493N7         0464FMT42       0493N7         0465505       0496STP4         0466XT023       0496STP4         0467202       0497SXR7         0468101       0498EHD4         0469UP27       0498EHD4		0472 000
0444	0443 3 03	0473X=Y50
0445-GT044       0475-LBL51         0446-LBL51       0476 m58         0447 C61       0477-CNT47         0448-GT044       0478-GT044         0449-FMT42       0479-LBL51         0450 505       0480- R68         0451-EEX26       0481-LBL-51         0452-FMT42       0482- m13         0453-FMT42       0483-XFR66         0455-E60       0485- 103         0457-FMT42       0486-FMT43         0457-FMT42       0487- 403         0459-303       0490-FMT43         0459-303       0490-FMT43         04610927       0492R63         0463606       0493M7         0464-FMT42       0494M5         0465505       0496STF4         0466XT023       0496STF4         0469STP4       0498END4         0469UP27		0474GTO44
0446-LBL51       0476 ff58         0447 C61       0477CNT47         0448-CNT47       0478-GTO44         0449-FMT42       0479-LBL51         0450 505       0480 ff68         0451-EEX26       0481-LBL51         0453-FMT42       0482 o13         0453-FMT42       0483-XFF67         0455 E60       0485 103         0455 E60       0485 103         0457FMT42       0487 4-06         0458STP41       0487 4-06         0459 303       0490FMT43         0461 UP27       0491FMT43         0463 606       0493 M7         0463 606       0493 M7         0463 606       0493 M7         0463 503       0496STP4         0465 503       0497S/R7         0468 101       0497S/R7         0468 101       0498END4         0469 UP27       0498END4		
0447 C61       0477CNT47         0448CNT47       0478GTO44         0449FMT42       0479LBL51         0450505       0480R63         0451EEX26       0481LBL51         0452FMT42       04820         0453FMT42       0483XFR63         0454		0476 n58
8448CNT47       9478GT044         9449FMT42       9479-LBL51         94595-05       9489BL51         9451EEX26       9481LBL51         9452FMT42       94829-13         9453FMT42       9483XFR67         94549		0477CNT47
0449-FMT42       0479-LBL51         0450-505       0480-A-63         0451-EEX26       0481-LBL51         0452-FMT42       0482- a-13         0453-FMT42       0483-XFR63         0455-E-60       0485-103         0456-C-61       0486-FMT43         0457-FMT42       0487-4-03         0458-STP41       0488-203         0459-303       0490-FMT43         0460-303       0490-FMT43         0463-607       0491-FMT43         0463-707       0492-A-7         0463-707       0493-N-7         0464-FMT42       0494-A-7         0465-707       0494-A-7         0466-XT023       0496-STP4         0467-2092       0497-SYR7         0468-101       0498-END4         04690707       0498-END4		9478GTO44
0450		0479LBL51
0451EEX26       0481LBL51         0452-FMT42       0482013         0453-FMT42       0483-XFR63         0454013       0485103         0455E60       0485103         0456C61       0486-FMT43         0457FMT42       0487403         0458STP41       0488203         0459303       0490-FMT43         0460303       0490-FMT43         0462707       0491FMT43         0463606       0493M7         0464FMT42       0494M5         0465505       0493M7         0466XTO23       0496STP4         0468101       0498EMD4         0469UP27		0480 A62
0452-FMT42       0482-0       -13         0453-FMT42       0483-XFR-63         0454-0       0485-1       -03         0455-E-60       0485-1      03         0456-C-61       0486-FMT-43       0487-4         0457-FMT42       0487-4       -03         0459-303       0489-XT023       0489-XT023         0460-303       0490-FMT43       0491-FMT43         0462-703       0491-FMT43       0492-R-63         0463-607       0493-N-7       0493-N-7         0464-FMT42       0493-N-7       0496-STP4         0465-505       0496-STP4       0496-STP4         0467-202       0498-EMD4         0468-101       0498-EMD4         04690727		
0453-FMT42       U483-XFR67         0454-0-013       U484-506         0455-E-60       U485-106         0456C-61       U486-FMT43         0457-FMT42       0487-406         0458-STP41       0488-206         0459-303       0490-FMT43         0460-303       0490-FMT43         0461UP27       0491FMT43         0463606       0493M6         0464FMT42       0494M5         0465505       0496STP4         0467202       0497SYR7         0468101       0498EMD4         0469UP27		10 10 100
0454       0      13       0484       5      01         0455       E      60       0485       1      01         0456       C      61       0486       FMT43         0457       FMT42       0487       4      02         0458       STP41       0488       2      03         0459       3      03       0499       XTO23         0460       3      03       0490       FMT43         0461       UP27       0491       FMT43         0463       6      06       0493       N      7         0463       6      06       0493       N      7         0464       FMT42       0494       N      7         0465       5      05       0496       STP4         0467       2      02       0497       SYR7         0468       1      01       0498       END4         0469       UP27       0498       END4		
0455       E60       0485       10.         0456       C61       0486-FMT4.         0457FMT42       0487       40.         0458STP41       0488       20.         0459       30.       0489XT02.         0460       30.       0490FMT4.         0461       0P27       0491FMT4.         0462       70.       0492		<u> </u>
0456 C61       0486FMT43         0457FMT42       0487 403         0458STP41       0488 203         0459 303       0489XT023         0460 303       0490FMT43         0461 UP27       0491FMT43         0462 707       0492 R63         0463 606       0493 M7         0463 606       0493 M7         0465 505       0495FMT4         0466XT023       0496STP4         0467 202       0497S/R7         0468 101       0498EMD4         0469 UP27		
0457FMT42       048740         0458STP41       048820         0459303       0489XT02         0460303       0490-FMT4         0461 UP27       0491FMT4         0462707       0492 R6         0463606       0493 N7         0464FMT42       0494 R5         0465505       0495FMT4         0466XT023       0496STP4         0467202       0497S/R7         0468101       0498END4         0469 UP27		
0458-STP41       0488-203         0459-303       0489-XT023         0460-303       0490-FMT43         0461- UP27       0491-FMT43         0462-707       0492- R6         0463-606       0493- N7         0464-FMT42       0494- N7         0465-505       0495-FMT4         0466-XT023       0496-STP4         0467-202       0497-SYR7         0468-101       0498-EMD4         0469- UP27		
0459 303	и458STP41	
0460 303       0490FMI4         0461 UP27       0491FMI4         0462 707       0492 R6         0463 606       0493 M7         0464FMT42       0494 R5         0465 505       0495FMT4         0466XT023       0496STP4         0467 202       0497S/R7         0468 101       0498EMD4         0469 UP27		
9461       UP27       9491       PMIMI4         9462       797       0492       R6         9463       696       9493       N7         9463       696       9493       N7         9463       795       9494       N5         9465       795       9495       PMI4         9466       792       9496       STP4         9468       191       9498       END4         9469       9498       END4	0460 3 03	
0463 606       0493 N7         0464FMT42       0494 05         0465 505       0495FMT4         0466XT023       0496STP4         0467 202       0497S/R7         0468 101       0498END4         0469 UP27	0461 UP27	
0463 606       0493 N7         0464FMT42       0494 05         0465 505       0495FMT4         0466XT023       0496STP4         0467 202       0497S/R7         0468 101       0498END4         0469 UP27	и462 707	
0465 505	0463 606	
0466XT023	0464FMT42	
0467 202	M465 5 W5	
0467 202	0466XT023	
0468 101 0498EHU4 0469 UP27	0467 202	
		0498END4
	0469 UP27	
	0470 XFR67	

22

23

24

	Table 28 Register Allocation For Revised 741 HP 9810A Program
a	CHANNEL COUNTER
b	SCRATCH AND INDIRECT
0	FREQUENCY, POWER COUNTER FOR DUMPING TO CASSETTE
1	LOSS FOR PORT 1
2	2
3	3
4	4
5	5
6	6
7	7
8	8
9	9
10	10
11	n
12	12
13	13
14	14
15	INCIDENT POWER COUPLER COEFFICIENT
16	REFLECTED POWER COUPLER COEFFICIENT
17	INPUT PORT
18	LOG V
19	CAL. FACTOR ADDRESS, V & I ADDRESSES
20	POWER COUNTER FOR PIN MODULATOR
21	DETECTOR COEFFICIENTS - B <sub>0</sub> & B <sub>1</sub> - DETECTOR # 1

DETECTOR 2

ASTRONAUTICS COMPANY - EAST

DETECTOR

B2 & B3 DETECTOR 1

B<sub>0</sub> & B<sub>1</sub>

	Table 28 (cont)		
25	DETECTOR COEFFICIENTS	- B <sub>0</sub> & B <sub>1</sub> -	DETECTOR # 3
26		B <sub>2</sub> & B <sub>3</sub>	3
27		B <sub>0</sub> & B <sub>1</sub>	4
28		B <sub>2</sub> & B <sub>3</sub>	4
29		B <sub>0</sub> & B <sub>1</sub>	5
30		B <sub>2</sub> & B <sub>3</sub>	5
31		B <sub>0</sub> & B <sub>1</sub>	6
32		B <sub>2</sub> & B <sub>3</sub>	6
33		B <sub>0</sub> & B <sub>1</sub>	7
34		B <sub>2</sub> & B <sub>3</sub>	7
35		B <sub>0</sub> & B <sub>1</sub>	8
36		B <sub>2</sub> & B <sub>3</sub>	8
37		B <sub>0</sub> & B <sub>1</sub>	9
38		B <sub>2</sub> & B <sub>3</sub>	9
39		B <sub>0</sub> & B <sub>1</sub>	10
40		B <sub>2</sub> & B <sub>3</sub>	10
41		B <sub>0</sub> & B <sub>1</sub>	11
42		B <sub>2</sub> & B <sub>3</sub>	11
43		B <sub>0</sub> & B <sub>1</sub>	12
44		B <sub>2</sub> & B <sub>3</sub>	12
45		B <sub>0</sub> & B <sub>1</sub>	13
46		B <sub>2</sub> & B <sub>3</sub>	13
47	,	B <sub>0</sub> & B <sub>1</sub>	14
48		B <sub>2</sub> & B <sub>3</sub>	14
49		B. & B.	15

```
Table 28 (cont)
      DETECTOR COEFFICIENTS - B2 & B3 - DETECTOR # 15
50
      VOLTAGE FOR PIN MODULATOR FOR POWER STEP # 1
51
                                                     2
52
                                                     3
53
54
                                                     5
55
 56
                                                     6
 57
                                                      8
 58
                                                     9
 59
                                                    10
 60
 61
                                                     11
                                                    12
 62
                                                    13
 63
                                                     14
 64
                                                     15
 65
                                                     16
 66
                                                     17
 67
                                                     18
 68
                                                     19
 69
                                                     20
 70
      TEMPORARY STORAGE FOR CALCULATING P
 71
 72
      SPARE
      POWER STEP TO ADD LARGE AMPLIFIER
 73
 74
      SPARE
 75
      SPARE
      S/N
 76
 77
      PIN
       CAL FACTOR
 78
 79
       VOUT
 80
       VOUT - VOUT
       VIII
 81
 82
       V<sub>ON</sub> #2
 83
       VON #2 - VON #2
 84
 85
       VON #6
```

### INTEGRATED CIRCUIT SUSCEPTIBILITY

MDC E1099 12 JULY 1974

Table 28 (cont)

HP 9830A Program to Convert from Data to Matrix Tapes for 741 COM FS[20,16], A REW. PROG. TO CONVERT FROM DATA TO MATRIX MAPE FOR 741 DISP FIRST MATRIX TAPE FILE #"; FOR K=1 TO 16
IF J+2\*I#1 THEN 170 DISP "FIRST FILE #"
INPUT H
FOR I=0 TO 9 Table 29 FOR I=0 TO 9

IOAD DATA M+I 100 IF I>0 I 120 IF A#C[1] 130 FOR J=1 140 FOR K=1 150 IF J+2\*I 160 IF K=2 I J+2\*I INI ", F4.0

IOOI

WRITE (15, 370)A FORMAT 30X, "S/N =", F7.0

PRINT

PORMAT

PRINT

HP 9830A Program to Convert from Data to Matrix Tape for 741 (cont) Table 29

WRITE (15,500)" 10c- VII III" FOR I=1 TO 20 WRITE (15,550)F[I,1],F[I,10],F[I,11],F[I,12],F[I,13],F[I,14],F[I,15],F[I,16] WRITE (15,400)" VONZ IONZ VONG"
FOR I=1 TO 20
WRITE (15,440)F[I,1],F[I,2],F[I,3],F[I,4],F[I,5],F[I,6],F[I,7],F[I,8],F[I,9]
FORMAT 5X,F9.4,F9.3,F8.3,F8.2,F7.2,F8.4,F8.2,F8.4,F8.2 VCC-", F4.0 100+ VCC+ III" TUON VONG" FORMAT 5X, 2F9.4, F7.2, 3F8.2, F9.4, F8.4 FOR I=1 TO 12 C.F. (DB) ION6 VII P(MW)
VON2 GOTO 80
DISP "S/N NOT ="A; C[1]
STOP
END PORFIAT PRINT NEXT I Q=Q+1 M=M+10 NEXT I ORMAT NEXT I STORE PRINT PRINT PRINT PRINT 

Table 30 741 Interference Data Plot Program from Matrix Tape (HP 9830A)

```
10 COM FS[20,16], A
20 REM PROGRAM TO PLOT 741 DATA FROM MATRIX TAPE
30 DISP "DATA COLUMN #":
40 INPUT Y
50 DISP "FIRST MATRIX FILE #":
60 INPUT X
70 DISP "YMIN.YMAX";
80 INPUT N.M
90 DISP "PLACE PAPER-PLATEN; CONT & EXEC"
100 STOP
110 SCALE 0,11,0,7.5
120 OFFSET 2.5.1.5
130 XAXIS 0, 1.4,0,7
140 YAXIS 0, 0.5, 0, 5
150 LABEL (*, 2, 3.4, PI/2, 5/7)
160 FOR J=0 TO 4
170 PLOT (IGT(2)+J)*1.4.0.1
180 CPIOT 0, -0.3
190 LABEL (*)"-";
200 PLOT (LGT(5)+J)*1.4.0.1
210 CPLOT 0, -0.3
220 LABEL (*)"-";
230 NEXT J
240 FOR I=1 TO 5
250 PLOT I*1.4,0,1
260 PLOT I*1.4,5,2
270 NEXT I
280 FOR I=1 TO 10
290 PLOT 0. I*0.5, 1
300 PLOT 7, I*0.5, 2
310 NEXT I
320 SCALE -53/14,57/14,N-1.5*(M-N)/5,N+6*(M-N)/5
330 FOR I=-2 TO 3
340 LABEL (*,1.5,1.7,0,5/7)
350 PLOT I,N,1
360 CPIOT -2,-2
370 LABEL (410, 1.5, 1.7, 0, 5/7) 10;
380 CPLOT 0, 0.6
390 LABEL (420, 1.125, 1.7, 0, 5/7) I;
400 NEXT I
410 FORMAT F3.0
420 FORMAT F2.0
430 LABEL (*,1.5,1.7,0,5/7)
440 J=(M-N)/5
450 FOR I=0 TO 5
460 PLOT -2, N+J*I, 1
470 CPLOT -9,-0.3
480 LABEL (500)N+J*I;
```

Table 30

741 Interference Data Plot Program from Matrix Tape (HP 9830A)

490 NEXT I

500 FORMAT F6.2

510 FOR K=1 TO 10

520 LOAD DATA X

530 LABEL (\*,1,0,8,0,5/7)

540 PLOT -2.07,F[1,Y],1

550 CPLOT -0.3,-0.3

560 LABEL (\*)"X"

570 FOR I=2 TO 20

580 IF LGT(F[I,1])>-2 THEN 600

590 F[I,1]=0.01

600 PLOT LGT(F[I,1]),F[I,Y],1

610 CPLOT -0.3,-0.3

620 LABEL (\*)"\*";

630 NEXT I

640 X=X+1

650 NEXT K

660 PLOT 0.2,M-1.7\*(M-N)/10,1

670 LABEL (\*)A

680 GOTO 90

690 END

### Table 31 4011 Interference Test Program (HP 9810A)

0000FMT42		
0001XFR67	0051 5 11	0101
0002XFR67	0051 911 0052L8L51	0101XFR67 0102IND31
0003 000	0053 B66	0103 b14
0004PNT45	0054FMT42	0103 814 0104FMT42
0005LBL51		
0006 A62	0055 404	0105 4 04
0007 101	0056 101 0057FMT42	0106 202
0008XT023	0058SFL54	0107XT023 0108PSE57
0009 202	9059FMT42	0109PSE57
0010 000	0060PSE57	0110PSE57
0011XFR67	0061CLX37	0111 1 01
0012 5 05	0062XTO23	0112XTO23
0013 505	0063 810	0113 a13
0014FMT42	0064 911	0114LBL51
0015 404	0065XT023	0115 D63
0016 202	0066 101	0116FMT42
0017XT023	0067 00A	0117 3 03
0018FMT42	0068 000	0118 303
0019FMT42	0069PSE57	011921
0020YT040	0070 101	0120 UPZ:
0021DIV35	0071XTO23	0121FMT42
0022 N73	0072 000	0122 4 04
0023FMT42	0073LBL51	0123 101
0024STP41	0074 C61	0124FMT42
0025XT023	0075FMT42	0125 101
0026 810	0076 404	0126FMT42
0027 606	.0077 101	0127 a13
0028PNT45	0078FMT42	0128 UP27
0029 UP27	0079 101	0129XFR67
0030EEX26	0080FMT42	0130 101
0031 303	0081XFR67	0131 911
0032DIV35	0082 707	0132X=Y50
0033 DN25	0083 505	0133 DN25
0034 UP27	0084 UP27	0134GTO44
0035INT64	0085XFR67	0135LBL51
003634	0086 202	0136 E68
0037 101	0087 000	0137 101
0038 000	0088X=Y50	0138 7 07
0039 X36	0089GTO44	0139XEY30
0040 DN25 0041INT64	0090SZR77	0140X>Y53
	0091LBL51	0141GTO44
0042 UP27	0092 L72	0142LBL51
0043 404 0044X=Y50	0093 505	0143 J75
0045 101	0094 404	0144CNT47 0145 DN25
0045 606	0095XFR67	0146 G15
0047 UP27	0096 +33 0097 202	0147EEX26
9048CNT47	0097 202	0148CHS32
9049YTO40	0099XTO23	0149 303
0050 101	0100 b14	0150X>Y53
	0100 014	କ୍ଷ୍ୟର ଓଡ଼ୀ ଅନ୍ତି

# Table 31 4011 Interference Test Program (HP 9810A)(cont)

0454 614 65		
0151 CLX37	0201 614	0251 1 01
0152XEY30	0202XFR67	
0153CNT47	0203IND31	0252 911
0154CNT47	0503IMD31	0253XFR67
	0204 614	0254 000
0155LBL51	0205 UP27	0255 UP27
0156 E60	0206INT64	
0157 DN25	020734	. 0256 101
0158 K55		0257 101
	0208 UP27	0258 X36
0159 404	0209EEX26	0259 707
0160XT023	0210 7 07	
0161 7 07	0211DIV35	9269 606
0162 707	0212RUP22	0261 +33
9163 a13		0262YT040
	0213XEY30	9263 b14
0164 UP27	0214XFR67	0264 DN25
0165 202	0215 707	
0166 X36	0216 707	0265YT040
0167 101		0266IND31
	0217 X36	0267 614
0168 911	0218 X36	0268GTO44
0169 +33	0219RUP22	
0170YT040	0220XEY30	0269LBL51
0171 b14	0221 X36	0270 I65
0172XFR67		0271LBL51
	0555 X36	0272 F16
0173IND31	0223 X36	0273 707
0174 614	0224 DN25	0274 810
0175 UP27	0225 +33	
0176INT64	0226 YE24	0275XEY30
017734		0276 101
	0227 +33	0277 101
0178 UP27	0228 707	0278XFR67
0179EEX26	0229 810	0279 X36
0180 505	0230 DN25	
0181DIV35	0231 K55	0280 000
0182 DN25		0281 +33
0183XEY30	0232 505	0282YT040
	0233 UP27	0283 707
0184 UP27	0234 101	0284 6 06
0185 101	0235 707	
0186 000	0236 UP27	0285 DN25
0187 X36	0237 a13	0286 YE24
		0287IND31
0188XFR67	0238X <y52< td=""><td>0288 X36</td></y52<>	0288 X36
0189 707	0239GTO44	0289 a13
0190 707	0240LBL51	
0191 X36	0241 F16	0290XFR67
0192 DN25		0291 101
	0242CNT4?	0292 911
0193 +33	0243 DN25	0293 UP27
0194YT040	0244XFR67	0294 a13
0195 707	0245 101	0295X=Y50
0196 810	0246 707	
0197PSE57	0247DIV35	0296RUP22
0198 101		0297GTO44
	0248 YE24	0298LBL51
0199XTO23	0249!ND31	0299 G15
0200 +33	0250DIV35	0300RHP22
CALL STREET, S		6966KIIF55

Table 31 4011 Interference Test Program (HP 9810A)(cont)

0301GTO44	0351XT023	0401IND31
0302LBL51	0352 +33	
0303 H74		0402 a13
	0353 707	0403XEY30
0304LBL51	0354 606	0404DIV35
0305 G15 (	0355 DN25	0405FMT42
0306XFR67		
	0356YTO40	0406FMT42
0307DIV35	0357IND31	0407 n56
0308 101	0358 707	0408CLX37
0309 810	0359 606	
		0409INT64
0310 UP27	0360GTO44	0410FMT42
0311 101	0361LBL51	0411PNT45
0312CHS32	0362 I65	
0313XFR67		0412 DN25
	0363LBL51	0413 K55
0314 +33	0364 K55	0414 404
0315 707	0365XFR67	0415 UP27
0316 606	0366 505	
0317XT023		0416 101
	0367 505	0417 000
0318 614	0368FMT42	0418 X36
0319 DN25	0369 4 04	0419 202
0320XT023	0370 2 02	0420 E60
0321IND31		
	0371\\T023	0421YT046
0322 614	0372FMT42	0422IND31
0323LBL51	-70373 484	0423 a13
0324 H'74	0374 1 01	0424 404
0325XT023	0375FMT42	
		0425 E60
0326IND31	0376SFL54 ,	0426XFR67
0327 +33	0377FMT42	0427IND31
0328 707	0378 101	A428 a13
0329 606	0379 101	The state of the s
0330LBL51		0429PHT45
	0380 UP27	0430 101
0331 I65	0381XFR67	0431XTO23
0332 101	0382 000	0432 +33
0333 E60	0383 X36	0433 0ติด
0334GTO44	0384 707	
		0434XT023
0335LBL51	0385 810 '	0435 +33
0336 D63 ,	0386 +33	0436 202
0337LBL51	0387YTO40	0437 000
0338 J75	0388 α13	0438XFR67
0339 202	0389XFR67	0439 000
0340 505	0390IND31	0440 UP27
0341XEY30	- 0391 α13	0441 303
0342 a13	0392CHS32	0442X>Y53
0343X)Y53		
	0393 UP27	0443GTO44
0344GTO44	0394 202	0444LBL51
0345LBL51	0395 D63	0445 C61
0346 K55	0396XFR67	0446CNT47
0347CNT47	0397IND31	
		0447FIIT42
0348PSE57	0398 n13	0448 505
0349PSE57	<b>0399 +</b> -33	0449EEX26
0350 101	040071040	0450FMT42
		w (www ) ) ) ) "Time

Table 31 4011 Interference Test Program (HP 9810A) (cont)

0451--FMT---42 0452-- a ---13 0453-- E ---60 0454-- C ---61 0455--IFG---43 0456--FMT---42 0457--STP---41 0458-- 2 ---02 0459-- 3 --- 03 0460-- UP---27 0461-- 8 --- 10 0462-- 6 --- ดิด 0463--FMT---42 0464-- 5 --- 05 0465--XT0---23 0466-- 2 ---02 0467-- 1 --- 01 0468-- UP---27 0469--XFR---67 0470-- 2 ---02 0471-- 0 ---00 0472--X=Y---50 0473--GTO---44 0474--LBL---51 0475-- A ---62 0476--CNT---47 0477--GTO---44 0478--LBL---51 0479-- B ---66 0480--LBL---51 0481-- L ---72 0482--XFR---67 0483-- 5 ---05 0484-- 5 ---05 0485--FMT---42 0486-- 4 --- 04 0487-- 2 --- 02 0488--XT0---23 0489--FMT---42 0490--FMT---42 0491-- A ---62 0492-- M ---70 0493-- # ---56 0494--FMT---42 0495---STP---41 0496--S/R---77 0497--END----46

Table 32 4011 Interference Test Program Register Allocations

- CHANNEL COUNTER
- SCRATCH & INDIRECT
- FREQUENCY (GHz), COUNTER FOR DUMPING TO CASSETTE
- LOSS FOR PORT 1

- INCIDENT POWER COUPLER COEFFICIENT
- REFLECTED POWER COUPLER COEFFICIENT
- INPUT PORT
- POWER COUNTER FOR PIN MODULATOR
- DETECTOR COEFFICIENTS BO & B3 DETECTOR # 1
- B2 & B3
- Bo & BI

25	DETECTOR	COEFFICIENTS	- B <sub>0</sub>	& B	1 -	DETECTOR	# 3
26			B <sub>2</sub>	& B	3		3
27			B <sub>0</sub>	& B	1		4
28			B <sub>2</sub>	& B	3		4
29			B <sub>O</sub>	& B			5
30			B <sub>2</sub>	& B	3		5
31			11-579	& B	0.30		6
32			51 103	& B	A 565		6
33				& B			7
34				& B	200		7
35				& B	100		8
36			10 000	& B	ALC: N		8
37				& B	<b>E</b> 010		9
38			TE COLUMN	& B	7		9
39			THE STATE OF	& B			10
40			100000	& B			10
41			99 (1)	& B			11
42				& B	11		11
43				& B	100		12
44				& B			12
45				& B	100		13
46				& B	THAT		13
47				& B			
48					A		14
				& B			14
49				& B	3.502		15
50			B <sub>2</sub>	& E	3		15

LOG V

77

Table 32 (cont)		
51 DETECTOR COEFFICIENT	S - B <sub>0</sub> & B <sub>1</sub> - DETECTOR #	16
52	B <sub>2</sub> & B <sub>3</sub>	16
53	B <sub>0</sub> & B <sub>1</sub>	17
54	B <sub>2</sub> & B <sub>3</sub>	17
55 VOLTAGE FOR PIN MODU	LATOR STEP # 1 (No RF)	
56	2	
57	3	
58	4	
59	5	
60	6	
61	7	
62	8	
63	9	
64	10	
65	11	
66	12	200
57	13	
68	14	
69	15	
70	16	
71	17	
72	18	
73	19	
74	20	
75 POWER STEP TO ADD L	ARGE AMPLIFIER	
76 CAL. FACTOR ADDRESS	, V ADDRESSES	

- 78 TEMPORARY STORAGE FOR CALCULATING P
- 79 BIAS UNIT REFLECTION LOSS COEFFICIENT
- 80 SPARE
- 81 SPARE
- 82 SPARE
- 83 SPARE
- 84 SPARE
- 85 SPARE
- 86 S/II
- 87 PDISS
- 88 PREF
- 89 CAL. FACTOR
- 90 V<sub>DD</sub>
- 91 V'DD
- 92 VOUT
- 93 VOUT
- 94 V<sub>SS</sub>
- 95 VIN
- 96 V<sub>IN2</sub>
- 97 VINI
- 98 PDISS
- 99 PREF
- 100 CAL. FACTOR
- 101 V<sub>DD</sub>
- 102 V<sub>DD</sub>
- 103 VOUT

104 VOUT

105 V<sub>SS</sub>

106 V'IN

107 VIN2

108 VIN1

=

ISS

VOUT

TOOI

4011 Data Tape to Matrix Tape Conversion Program (HP 9830A) Table 33

4011 Data Tape to Matrix Tape Conversion Program (HP 9830A)(cont) Table 33

(15,3%)" IINRE VINZ VIN1"
1 TO 20
(15,450)F[I,1],F[I,2],F[I,3],F[I,4],F[I,5],F[I,6],F[I,7],F[I,8],
(15,460)F[I,9],F[I,10],F[I,11] O FORWAT F9.3, F8.3, F6.2, 2F6.3, F7.3, F6.3, F6.2
O FORMAT 3F7.3
O GOTO 500
O INSP "S/N NOT = "A;C[1]
O INSP "CHANGE TO MATRIX TAPE";
O STOP
O STOP
O STOP
O STORE DATA Q
O FM.+10 Q=Q+1 DISP "CHANGE TO DATA TAPE"; STOP GOTO 80 NEXT I RITE RITE WRITE PRINT PRINT PRINT PRINT 

### Table 34

General Plot Program from Matrix Tape For 4011

```
10 COM FS[23.11].A
20 MAT F= ZER
30 DISP "FOR PLOT. WRITE COL# & PRESS EXEC";
40 INPUT K
50 DISP "FIRST MATRIX FILE NO.":
60 INPUT Q
70 SCALE 0,8.5,0,10
80 OFFSET 2,1.5
90 XAXIS 0, 1.5, 0,6
100 YAKIS 0,0.7,0,7
110 FOR J=0 TO
120 PLOT (LGT(2)+J)*1.5,0,1
130 LABEL (*,1,3.4,PI/2,7/6)
140 CPLOT 0,-0.3
150 LABEL (*)"-";
160 PLOT (LGT(5)+J)*1.5,0,1
170 CPTOT 0,-0.3
180 LABEL (*)"-";
190 NECT J
190 NEXT J
200 DISP "YMIN, YMAX";
210 INPUT N, M
220 SCALE -7/3, 10/3, N-1.5*(M-N)/7, N+8.5*(M-N)/7
230 FOR I=-1 TO 3
240 LABEL (*,1.5,1.7,0,7/6)
250 PLOT I,N,1
260 CPLOT -2,-2
270 LABEL (310,1.5,1.7,0,7/6)10;
280 CPLOT 0.0.6
290 LABEL (320,1.125,1.7,0,7/6)I;
300 NEXT I
310 FORMAT F3.0
320 FORMAT F2.0
330 LABEL (*,1.5,1.7,0,7/6)
340 A=(M-N)/5
350 FOR I=0 TO 5
360 PLOT -1, N+A*I, 1
370 CPLOT -7,-0.3
380 LABEL (400)N+A*I;
390 NEXT I
400 FORMAT F7.3
410 IABEL (*,1,0.8,0,7/6)
420 FOR G=Q TO Q+4
430 LOAD DATA G
440 FOR I=1 TO 20
450 F[1,1]=0.1
460 PLOT LGT(F[1,1]), ABS(F[1,K]),1
470 CPLOT 0.3,-0.3
```

Table 34 General Plot Program from Matrix Tape for 4011 (cont)

480 LAHEL (\*)"\*"
490 IPLOT 0,0,1
500 NEXT I
510 NEXT G
520 PEN
530 SCALE 0,8.5,0,10
540 OFFSET 2,1.5
550 FOR I=1 TO 4
560 PLOT I\*1.5,0,1
570 PLOT I\*1.5,7,2
580 NEXT I
590 FOR I=1 TO 10
600 PLOT 0,I\*0.7,1
610 PLOT 6,I\*0.7,2
620 NEXT I
630 PEN
640 GOTO 30

0149-- b ---14

0156-- UP---27

0049--LBL---51

0050-- B ---66

### Table 35 2002 Hybrid Interference Test Program (HP 9810A) 8601 | 11 --- - 20 0001- | ---55 0002--CLX---37 0051 -- FHT --- - 42 0101--- 177---42 0052-- 4 --- 04 0102-- a ---13 1803--FMT---42 0053-- 1 ---01 0103-- UP---27 0004--XFR---67 0054--FMT---42 0104--XFR---67 0005--XFR---67 0055--SFL---54 0105-- 1 --- 01 0006-- 0 ---00 0106-- 9 ---11 0056--FMT---42 0007--PNT---45 0057--CNT---47 0107--X=Y---50 9008---LBL---51 0058--FMT---42 0108-- DN---25 0009-- A ---62 0059--FMT---42 0109--GTO---44 9018--CNT---47 0060--YT0---40 0110--LBL---51 0011-- 1 ---01 0012-- 6 ---06 0061-- E ---60 0111-- E ---60 0062--XT0---23 0112-- 1 ---01 0013--XT0---23 0063--CNT---47 0113-- 7 ---07 0014-- 2 ---02 0064-- π ---56 0114--XEY---30 0015-- 0 ---00 0065-- 0 ---71 0115--X>Y---53 0016--CNT---47 0066--IND---31 0116--GTO---44 0017-- 1 ---01 0067-- E ---60 0117--LBL---51 0918--XT0---23 0068-- a ---13 0118-- J ---75 0019-- 0 ---00 0069--FMT---42 0119--CNT---47 0020--FMT---42 0070--CNT---47 0120-- DN---25 0021--FMT---42 0071--STP---41 0121-- G ---15 0022-- I ---65 0072--CLX---37 0122--EEX---26 0023-- N ---73 0073--XT0---23 0123--CHS---32 0024-- n ---56 0074-- 7 ---07 0124-- 3 --- 03 0075-- 5 ---05 0025--1/8---17 0125--X>Y---53 0026--XT0---23 0076--PSE---57 0126--CLX---37 0027--CNT---47 0077--FMT---42 0127--XEY---30 ผม28-- ๙ ---56 0078-- 4 ---04 0128---CNT----47 0029-- 0 ---71 0079-- 1 ---01 0129--CNT---47 0030-- a ---13 0080--FMT---42 0130--LBL---51 0031--XT0---23 0081-- 1 ---01 .0131-- E ---68 0032--FMT---42 0082--FMT---42 0132-- DN---25 0033--STP---41 0083--PSE---57 0133-- K ---55 0034--XT0---23 0084--PSE---57 0134-- 4 --- 04 0085--PSE---57 0035-- 1 ---01 0135--XT0---23 0036-- 9 ---11 0086-- 1 ---01 0136-- 5 ---05 0037--PNT---45 0087--XT0---23 0137-- 7 ---07 0038--FMT---42 0088-- a ---13 0138-- a ---13 0089--LBL---51 0039--FMT---42 0139-- UP---27 0040--YT0---40 0090-- D ---63 0140-- 2 ---02 0141-- X ---36 0091--FMT---42 0041--DIV---35 0042-- N ---73 0092-- 3 ---03 0142-- 1 ---01 0043--FMT---42 0093-- 3 ---03 0143-- 9 ---11 0094-- . ---21 0095-- UP---27 0044--STP---41 0144-- + ---33 ы045--XT0---23 0145--YT0---40 0046-- 7 ---07 0047-- 3 ---03 0096--FMT---42 0146-- 6 ---14 0097-- 4 ---04 0147--XFR---67 0048--PNT---45 0098-- 1 ---01 0148--IND---31

0099--FMT---42

0100--- 1 ----01

# Table 35 2002 Hybrid Interference Test Program (HP 9810A)(cont)

0151(NT64	0004 11 04	0054 NIII 00
015234	0201 - 71 24	0251RUP22
	0202 +33	025257044
0153 UP27	0203 505	0253LBL51
0154EEX26		
	0204 810	0254 H74
0155 505	0205 DN25	0255LBL51
0156DIV35	0206 K55	0256 G15
0157 DN25		
	0207 505	0257XFR67
0158XEY30	0208 UP27	0258DIV35
0159 UP27		
	0209 101	0259 101
0160 101	0210 707	0260 810
0161 000	0211 UP27	
0162 X36		0261LBL51
	0212 a13	0262 H74
0163XFR67	0213X <y52< td=""><td>0263 UP27</td></y52<>	0263 UP27
0164 505		
	0214GTO44	0264 707
0165 707	0215LBL51	0265 505
0166 X36	0216 F16	0266XFR67
0167 DN25		
	0217CNT47	0267 +33
0168 +33	0218 DN25	0268 a13
0169YTO40		
	0219XFR67	0269XT023
0170 505	0220 101	0270 614
0171 810	0221 707	0271YT040
0172PSE57		
	0222DIV35	0272IND31
0173 101	0223 YE24	0273 b14
0174XT023	0224IND31	0274YTO40
0175 +33		
	0225DIV35	0275 +33
0176 b14	0226 101	0276 707
0177XFR67		
	0227 911	0277 505
0178IND31	0228YT040	0278LBL51
0179 614	0229 911	0279 I65
0180 UP27		
	0230 202	0280 101
0181INT64	0231GTO44	0281 E60
018234	0232LBL51	0282GT044
0183 UP27		
	0233 I65	0283LBL51
0184EEX26	0234LBL51	0284 D63
0185 707	0235 F16	0285LBL51
0186DIV35		
	0236 DN25	0286 J75
0187RUP22	0237 YE24	0287 101
0188XEY30		
	0238IND31	0288 707
0189XFR67	0239 X36	0289XFR67
0190 505	0240 a13	0290 +33
0191 707		
	0241XFR67	0291 202
0192 X36	0242 101	0292 000
0193 X36	0243 911	0293XEY30
0194RUP22	0244 UP27	0294 a13
0195XEY30	0245 a13	0295X>Y53
0196 X36		
	0246X=Y50	0296GTO44
0197 X36	0247RUP22	0297LBL51
0198 X36	0248GT044	0298 K55
0199 DN25		
	0249LBL51	0299CNT47
		The said has been been been been seen
0200 +33	0250 G15	0300PSE57

# Table 35 2002 Hybrid Interference Test Program (HP 9810A)(cont)

8301 - PSE57	DOME !	mana me
	0351	0401 EER26
0302 707	0352 606	0402 3 03
0303 505	0353CNT47	0403 X36
0304XEY30		
	0354 911	0404YT040
0305 a13	0355 707	0405IND31
0306 +33	0356XT023	0406 a13
0307YT040	0357 α13	0407 101
U308 b14	0358LBL51	0408 E60
0309 DN25	0359 L72	0409 YE24
0310YT040		
	0360XFR67	0410IND31
0311IND31	0361IND31	0411 a13
0312 h14	0362 α13	0412EEX26
0313GTO44		
- · · · · · · · · · · · · · · · · · · ·	0363 UP27	0413 303
0314LBL51	0364 101	0414 X36
0315 I65	0365 E60	0415YT046
0316LBL51		
	0366XFR67	0416IND31
0317 K55	0367IND31	0417 a13
0318FMT42	0368 α13	.0418 101
0319 4 04	0369CNT47	0419 E60
0320 101		
	037034	0420 YE24
0321FMT42	0371 101	0421IND31
8322SFL54	0372 000	0422 α13
0323FMT42		
	0373 X36	0423EEX26
0324XFR67	0374YT040	0424 303
0325 911	0375IND31	0425 X36
0326 303		
	0376 α13	0426YT040
0327 UP27	0377 101	0427IND31
0328XFR67	0378 E60	0428 a13
0329 911	0379 101	0429XFR67
й330 404		
	0380 000	0430 707
033134	0381 505	0431 5 05
03 <b>32 202</b>	0382 UP27	0432CHS32
0333 000	0383 a13	0433 UP27
0334 X36	0384X <y52< td=""><td>0434XFR67</td></y52<>	0434XFR67
0335YT040	0385GTO44	0435 911
0336 911	0386LBL51	0436 202
0337 404		
	0387 L72	0437 +33
0338XFR67	0388CNT47	0438YTO40
0339 911	0389CNT47	0439 707
0340 505	0390XFR67	0440 4 04
0341 UP27	0391IND31	9441XEY30
0342XFR67	0392 o13	0442DIV35
0343 911	0393 UP27	0443FMT42
0344 6 06		
	0394 101	0444FMT42
034534	0395 E60	0445 π'56
0346 101	0396XFR67	0446CLX37
0347 000	0397IND31	0447INT64
0348 000	0398 a13	0448FNT42
0349 X36	0399CNT47	0449PNT45
0350YT040	040034	0450 DH25
The state of the s		a time in the fine in

Table 35 2002 Hybrid Interference Test Program (HP 9810A)(cont)

0451	10 55
0452	4 94
0453	UP27
0454	101
0455	000
0456	X36
0457	YT040
0458	7 97
0459	7 07 5 05
9469	XFR67
0461	911
0462	911 303
0463	PNT45
9464	XFR67
0465	101 000
0466	000
0467	6 96
9468	ÜP27 FMT42
0469	FMT42
0470	505
9471	EEX26
0472	FMT42
0473	FMT42
0474	a13
0475	E60
0476	061
0477	071
0478	
0479	D63

0400 · 11147 04811742
048142
048257841
0483 303
0483 303 0484 606
0495 HP27
0486 7 07
0487 303
0486 707 0487 303 0488FMT42
9489 5 05
0490XT023
0491 101
0492XT023
0493 +33
0494 000
U495XFR67
0496 000
0497 UP27
0438 511
0499X>Y53
8500GTO44
0501LBL51
0501LBL51 0502 B66 0503CNT47 0504GT044
0503CNT47
0504GTO44
0506 A62
0507STP41
and here, and the same on the first and many of the

Table 36 General Device and 2002 Interference Test Register Allocations

- a CHANNEL COUNTER
- b SCRATCH AND INDIRECT
- O FREQUENCY (GHz), INTERFERENCE LEVEL COUNTER
- 1 LOSS FOR PORT 1
- 2
- 3
- 4
- 5
- 5
- ,

8

- 8
- 9
- 10 10
- 11
- 12
- 13
- 14
- 15
- 16
- 17 INCIDENT POWER COUPLER COEFFICIENT
- 18 REFLECTED POWER COUPLER COEFFICIENT
- 19 INPUT PORT
- 20 NUMBER OF DC PARAMETERS TO BE MONITORED
- 21 DETECTOR COEFFICIENTS B<sub>0</sub> & B<sub>1</sub> DETECTOR # 1
- B<sub>2</sub> & B<sub>3</sub>
- $B_0 & B_1$  2

Table 36 (cont)

	Table 36 (cont)		
24	DETECTOR COEFFICIENTS -	- B2 & B3 - DETECTOR #	2
25		B <sub>0</sub> & B <sub>1</sub>	3
26		B <sub>2</sub> & B <sub>3</sub>	3
27		B <sub>0</sub> & B <sub>1</sub>	4
28		B <sub>2</sub> & B <sub>3</sub>	4
29		B <sub>0</sub> & B <sub>1</sub>	5
30		B <sub>2</sub> & B <sub>3</sub>	5
31		B <sub>0</sub> & B <sub>1</sub>	6
32		B <sub>2</sub> & B <sub>3</sub>	6
33		B <sub>0</sub> & B <sub>1</sub>	7
34		B <sub>2</sub> & B <sub>3</sub>	7
35		B <sub>0</sub> & B <sub>1</sub>	8
36		B <sub>2</sub> & B <sub>3</sub>	8
37		B <sub>0</sub> & B <sub>1</sub>	9
38		B <sub>2</sub> & B <sub>3</sub>	9
39		B <sub>0</sub> & B <sub>1</sub>	10
40		B <sub>2</sub> & B <sub>3</sub>	10
41		B <sub>0</sub> & B <sub>1</sub>	11
42		B <sub>2</sub> & B <sub>3</sub>	11
43		B <sub>0</sub> & B <sub>1</sub>	12
44		B <sub>2</sub> & B <sub>3</sub>	12
45		B <sub>0</sub> & B <sub>1</sub>	13
46		B <sub>2</sub> & B <sub>3</sub>	13
47		B <sub>0</sub> & B <sub>1</sub>	14
48		B <sub>2</sub> & B <sub>3</sub>	14
49		B <sub>0</sub> & B <sub>1</sub>	15

Table 36 (cont)

50	DETECTOR COEFFICIENTS	- B <sub>2</sub>	&	B <sub>3</sub>	- DETECTOR	#	15
51		Bo	&	В			16
52		B <sub>2</sub>	&	B <sub>3</sub>			16
53		Bo	&	B <sub>1</sub>			17
54		B <sub>2</sub>	&	B <sub>3</sub>			17

- 55 LOSS WITH OLD HP BIAS UNIT AND FIXTURE
- 56 SPARE
- 57 LOG V
- 58 TEMPORARY STORAGE FOR CALCULATING P
- 59 SPARE
- 60 SPARE
- 61 SPARE
- 62 SPARE
- 63 SPARE
- 64 SPARE
- 65 SPARE
- 66 SPARE
- 67 SPARE
- 68 SPARE
- 69 SPARE
- 70 SPARE
- 71 SPARE
- 72 SPARE
- 73 S/N
- 74 PDISS
- 75 CAL. FACTOR

```
Table 36 (cont)
76
77
78
79
80
81
82
83
84
             9
85
             10
86
             11
87
             12
88
             13
89
             14
90
             15
91
             16
            PINC
92
            V<sub>OUT 1</sub> (VOLTAGE MONITORED ON PRINTER) (V<sub>COLL</sub> - 2002)
93
            I<sub>OUT 1</sub> (I<sub>COLL</sub> - 2002)
94
            V<sub>OUT 2</sub> (V<sub>BASE</sub> - 2002)
95
96
            IOUT 2 (NOTHING - 2002)
            V<sub>IN 1</sub> (V<sub>IN 9</sub> - 2002)
97
            I<sub>IN 1</sub> (I<sub>IN 1 + 2</sub>)
98
            VIN 2 (VIN 1 + 2)
99
           I<sub>IN 2</sub> (I<sub>IN 1 + 2</sub>)
100
101
            YIN 3
```

Table 36 (cont)

102 I<sub>IN 3</sub>

103 V<sub>IN 4</sub>

104 I<sub>IN 4</sub>

105 V<sub>CC</sub>

106 I<sub>CC</sub>

107 I<sub>GND</sub>

108 SPARE (I<sub>EMIT</sub> ON 2002)

.20]

2002 Hybrid Data Reduction Program (HP 9830A) Table 37

",F3.0, "RF LEVEL" , "F3.0, "RF LEVEL ", F3.0, "RF LLIVEL PARANIZER ", I+0, I+1, I+2, I+3 P INC. P DIS. C.F. WRITE (15,230)S FORMAT 35X,"S/N =",F5.0 FORMAT 4F13.4,F1.1
FOR I=0 TO 4 STEP 4
FORMAT F3.0, "RF LEVEL
WRITE (15, 270)" P 920 UIM A[8,36], C[36] 10 DIM A[8, 36], C[36 20 DISP "FILE #"; 30 INPUT M 40 FOR K=0 TO 7 50 I=0 60 IOAD DATA M+K C 70 IF K#0 THEN 110 80 C[3]=0 90 S=C[1] 正 時 1 元 130 THEN 8 FOR J=1 TO E PRINT NEXT J TF S#C[1] FOR J= 1 TAIL J ]= NEXT J WRITE WRITE VRITE PRINT NEXT K PRIM PRIM 

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Table 37 2002 Hybrid Data Reduction Program (cont)

44444444444444 22228282828282828 FORMAT F5.0, 1X, 4F13. 4, F1.1 [1,K+3], A[2,K+3], A[3,K+3], A[4,K+3] MRITE (15, 360)" P", K, A[1,K+3], A[2,K+3], A[3,K+3] INC. ",A[1,20],A[2,20],A[3,20],A[4,20] 222282228282824E I+2, 1+2 1+2 1+2 1+2 =";S;C[1] M=M+8 GOTO 40 DISP "S/N NOT : STOP END FOR K=1 TO 16 FOR K=1 PRIM NEXT K FOR K= NEXT K NEXT K WRITE WRITE WRITE WRITE WRITE WRITE PRINT WRITE WRITE WRITE WRITE WRITE WRITE WRITE PRINT WRITE WRITE 

Table 38	Extra Digital Device Interference	Test Program (HP 9810F)	
######################################			
пон1 к55	0051 101	0101 · F · E57	
0002CLX37	0052 311	010201	
0008FMT42	0053PNT45	0103+-XTO23	
0604XFR67	0054FMT42	0104 α13	
0005XFR67	0055FMT42	0105L8L51	
0006 0 00	0056YT040	0106 D63	
0007PNT45	0057DIV35	0107FMT42	
0008LBL51	0058 N73	0108 303	
0009 A62	0059FMT42	0109 303	
0010CNT47	0060STP41	011021	
0011CNT47	0061XT023	9111 UP27	
0012CNT47	0062 707	0112FMT42	
0013CNT47 0614CNT47	0063 303	0113 404	
0015CNT47	0064PNT45	0114 101	
0016ENT47	0065LBL51 0066 B66	0115FMT42 0116 101	
0017CNT47	0067FMT42	0117FMT42	
0018CNT47	0068 4 04	0118 a13	
0019CNT47	0069 101	0119 UP27	
0020CNT47	0070FMT42	0120XFR67	
0021CNT47	0071SFL54	0121 101	
0022CNT47	0072FMT42	0122 911	
0023CNT47	0073CNT47	0123X=Y50	
6624CNT47	0074FMT42	0124 DN25	
0025CHT47	0075FMT42	0125GTO44	
0026CNT47	0076YTO40	0126LBL51	
0027 101	0077 E60	0127 E60	
ии28 6 <b>0</b> 6	0078XT023	0128 101	
0029XT023	0079CNT47	0129 707	
0030 202	. 0080 и56	0130XEY30	
0931 000	0081 071	0131X>Y53	
0032CNT47	0082IND31	0132GTO44	
0033 101	0083 E60	0133LBL51	
0034XT023 0035 000	0084 α13 0085FMT42	0134 J75 0135CNT47	
0036FMT42	0086CNT47	0136 DN25	
0037FMT42	0087STP41	0137 G15	
0038 I65	0088CLX37	0138EEX26	
₩039 N73	0089XTO23	0139CHS32	
0040 r56	0090 707	0140 303	
06411/X17	0091 505	0141X>Y53	
0042XT023	0092PSE57	0142CLX37	
0043CNT47	0093FMT42	0143XEY30	
0044 n56	0094 404	0144CNT47	
0045 071	0095 101	0145CNT47	
ий46 а13	0096FMT42	0146LBL51	
0047XT023	0097 101	0147 E60	
0048FMT42	0098FMT42	0148 DN25	
0049STP41	0099PSE57	0149 K55	4
0050 XTO23	0100PSE57	0150 404	

### Table 38 Extra Digital Device Interference Test Program (HP 9810A)(cont)

	Total Control of the	
0:514:023	0201-707	925: F16
0152 505	0202 - PIV35	
		0252 3125
0153 707	0203RUP22 .	0253 YE24
0154 o13	0204XEY30	0254IND31
0155 UP27	0205XFR67	0255 X36
0156 202		650011 V 11106
	0206 5·-4-05	Ø256 α13
0157 X36	0207 707	0257XFR67
0158 101	0208 X36	0258 101
0159 911	0209 X36	
		0259 911
0160 +33	0210RUP22	0260 UP27
0161YTO40	0211XEY30	0261 a13
0162 614	0212 X36	0262X=Y50
0163XFR67		
	0213 X36	0263RUP22
0164IND31	0214 X36	0264GTO44
0165 b14	0215 DN25	0265LBL51
0166 UP27	0216 +33	0266 G15
0167INT64	0217 YE24	0267RUP22
016834	0218 +33	0268GT044
0169 UP27	0219 505	0269LBL51
0170EEX26	0220 810	0270 H74
0171 5 05		
	0221 DN25	0271LBL51
0172DIV35	0222 K55	0272 G15
0173 DN25	0223 505	0273XFR67
0174XEY30	0224 UP27	0274DIV35
0175 UP27		
	0225 101	0275 101
0176 101	0226 707	0276 810
0177 000	0227 UP27	0277LBL51
0178 X36	0228 a13	0278 H74
0179XFR67	0229X(Y52	
		0279 UP27
0180 505	0230GTO44	0280 707
0181 707	0231LBL51	0281 505
0182 X36	0232 F16	0282XFR67
0183 DN25	0233CNT47	0283 +33
0184 +33		
	0234 DN25	0284 a13
0185YTO40	0235XFR67	0285XT023
0186 505	0236 101	0286 ь14
0187 810	0237 707	0287YT040
0188PSE57		
	0238DIV35	0288IND31
0189 101	0239 YE24	0289 b14
0190XT023	0240IND31	0290YT040
0191 +33	0241DIV35	0291 +33
0192 614		
	.0242 101	0292 707
0193XFR67	0243 911	0293 505
0194IND31	0244YT040	0294LBL51
0195 b14	0245 911	0295 I65
U196 UP27	0246 202	
		0296 101
0197INT64	0247GTO44	0297 E60
019834	0248LBL51	0298GT044
0199 UP27	0249 I65	0299LBL51
0200EEX26	0250LBL51	
"of how "of "of the heat"   Company of the Company of the heat of the company of	egoe Lot. Tot	0300 D63

## Table 38 Extra Digital Device Interference Test Program (HP 9810A)(cont)

and the second of the second o	GOE 1 11 CG	0441 1140
. 0301 - LDL51	035: E60	
0302 J75	935267	040 IHD31
		0403 a13
0303 101	0353IND31	
0304 707	0354 a13	0404XFR67
U305XFR67	0355CNT:47	0405 707
		0406 505
U306 +33	035634	
0307 202	0357 101	0407CHS32
		0408 UP27
0308 000	0358 000	
0309XEY30	0359 X36	0409XFR67
9319 a13	0360YTO40	0410 911
		0411 202
0311X>Y53	0361IND31	0411 - 25
0312GTO44	0362 α13	0412 +33
		0413YT040
0313LBL51	0363 101	
0314 K55	0364 E60	0414 707
0315CNT47	0365 101	0415 404
0316PSE57	.0366 000	. 0416XEY30
0317PSE57	0367 505	0417DIV35
		0418FMT42
0318 707	0368 UP27	
0319 505	0369 a13	0419FMT42
		0420 n56
0320XEY30	0370XKY52	
H321 013	0371GTO44	. 0421CLX37
		0422INT64
U322 +33	0372LBL51	
0323YTO40	0373 L72	0423FMT42
		0424PNT45
0324 ь14	0374CNT47	
0325 DN25	0375CNT47	0425 DN25
		0426 K55
0326YTO40	0376XFR67	
0327IND31	0377IND31	0427 404
0328 b14	0378 a13	0428 UP27
0329GT044	0379 UP27	0429 101
0330LBL51	0380 101	0430 000
9331 I65	0381 E60	0431 X36
0332LBL51	0382XFR67	0432YT040
0333 K55	0383IND31	0433 707
Magages M seran		
0334FMT42	0384 a13	0434 505
изз5 404	0385CNT47	0435XFR67
		0436 911
0336 101	038634	
0337FMT42	0387EEX26	0437 303
0338SFL54	-03 <b>88</b> 3 <b></b> 03	0438PNT45
	0389 X36	0439XFR67
0339FMT42		
0340 911	0390YT040	0440 101
	0391IND31	0441 000
0341 303		
0342XTO23	0392 a13	0442 606
	0393 101	0443 UP27
0343 a <u>1</u> 3 .		
0344LBL51	0394 E60	0444FMT42
	0395 YE24	0445 505
0345 L72		
0346XFR67	0396IND31	0446EEX26
	0397 a13	0447FMT42
0347IND31		
0348 a13	0398EEX26	0448FMT42
	0399 303	0449 a13
0349 UP27		
0350 101	0400 %36	0450 F60

Table 38 Extra Digital Device Interference Test Program (HP 9810A) (cont)

0451 - 0 ---61 0452-- 0 ---71 0453-- a ---13 0454-- D ---63 0455--CNT---47 0456---FMT----42 0457--STP---41 0458-- 3 ---03 0459-- 6 ---06 9460-- UP---27 0461-- 7 ---07 0462-- 3 ---03 8463--FMT---42 0464-- 5 --- 05 0465--XT0---23 0466-- 1 ---01 0467--XTO---23 0468-- + ---33 0469-- 0 ---00 0470--XFR---67 0471-- 0 ---00 0472-- UP---27 0473-- 5 --- 05 3474--X>Y---53 0475--GTO---44 0476--LBL---51 0477-- B ---66 0478--CNT---47 0479--GTO---44 0480--LBL---51 8481-- A ---62 0482--STP---41 0483--END --- 46 Extra Digital Device Data Reduction and Print

INPUT II

RF LEVEL" FORMER F5.0.1X, 4F13.4, F1.1 [1, K+3], A[2, K+3], A[3, K+3], A[4, K+3] NEXT K ", A[1,20], A[2,20], A[3,20], A[4,20] LEVEL A 5 4 2, 2 1 A 3, 1 A 4, 1 A 5 4 2, 3 A 3, 3 A 4, 2 2 LEVEL 띮 LEVEL P DIS. IIIG. 55551 0 AHAHA (15,160) FOR K=0 TO 3

LOAD DATA H+K, C

FOR J=1 TO 36

IF K#O THEN 90

C[3]=0

A[K+1,J]=C[J]

NEXT I

NEXT I

O NEXT I

O NEXT I

O NEXT I

O NEXT I

O NEXT J

NEXT I

O NEXT J

NEXT I

O NEXT J

NEXT J

NEXT I

NEXT J

NE (15,150)" (15,150)" (15,150)" 22222 15,150)" FOR K=1 TO 16 v.v.v.v. PRINT ( WRITE WRITE SELECTION OF SELEC PRINT  Table 39 Extra Digital Device Data Reduction and Print (cont)

I IN 1 ", A 1, 26 , A 2, 26 , A 3, 26 , A 4, 26 I I IN 2 ", A 1, 27 , A 2, 27 , A 3, 27 , A 4, 27 I IN 2 ", A 1, 29 , A 2, 28 , A 3, 29 , A 4, 29 I IN 3 ", A 1, 30 , A 2, 30 , A 3, 30 , A 4, 30 I IN 4 ", A 1, 32 , A 2, 32 , A 3, 33 , A 4, 32 I GC ", A 1, 35 , A 2, 35 , A 3, 35 , A 4, 35 I GC ", A 1, 35 , A 2, 35 , A 3, 35 , A 4, 35 I GC ", A 1, 35 , A 2, 35 , A 3, 35 , A 4, 35 I GC ", A 1, 35 , A 2, 35 , A 3, 35 , A 4, 35 I GND ", A 1, 35 , A 2, 35 , A 3, 35 , A 4, 35

340 WRITE (15,150)"
350 WRITE (15,150)"
370 WRITE (15,150)"
380 WRITE (15,150)"
400 WRITE (15,150)"
420 WRITE (15,150)"
430 WRITE (15,150)"
440 FOR K=1 TO 17
450 PRINT
460 INEXT X
470 M=M+4
480 GOTO 40

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#### RELATED DOCUMENTS

- 1. MDC E0595, "Integrated Circuit Electromagnetic Susceptibility Investigation Study Phase Report " dated 5 May 1972.
- 2. MDC E0690, "Integrated Circuit Electromagnetic Susceptibility Investigation Development Phase Report" dated 19 October 1972.
- 3. MDC E0883, "Integrated Circuit Electromagnetic Susceptibility Investigation Interim Report No. 1" dated 24 August 1973.
- 4. MDC E0981, "Integrated Circuit Electromagnetic Susceptibility Investigation Interim Report No. 2" dated 28 December 1973.
- 5. MDC E1099, "Integrated Circuit Electromagnetic Susceptibility Investigation Test and Measurement Systems" dated 12 July 1974.
- 6. MDC E1101, "Integrated Circuit Electromagnetic Susceptibility Investigation MOS NAND Gate Study" dated 26 July 1974.
- 7. MDC E1102, "Integrated Circuit Electromagnetic Susceptibility Investigation Pulse Interference Study" dated 12 July 1974.
- 8. MDC E1103, "Integrated Circuit Electromagnetic Susceptibility Investigation Package Effects Study" dated 12 July 1974.
- 9. MDC E1123, "Integrated Circuit Electromagnetic Susceptibility Investigation Bipolar NAND Gate Study" dated 26 July 1974.
- 10. MDC E1124, "Integrated Circuit Electromagnetic Susceptibility Investigation Bipolar Op Amp Study" dated 9 August 1974.
- 11. MDC E1125, "Integrated Circuit Electromagnetic Susceptibility Investigation MOS/Hybrid Study" dated 9 August 1974.
- 12. MDC E1126, "Integrated Circuit Electromagnetic Susceptibility Investigation Susceptibility Survey Study" dated 9 August 1974.

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